Government Girls' Polytechnic, Bilaspur

Name of the Lab: **Electronics Lab**

Practical: **Analog Electronics Lab**

Class : **4th Semester (ET&T)**

Teachers Assessment: 10 End Semester Examination: 50

EXPERIMENT NO. – 01

1.OBJECTIVE : - (a)Measurement of Different Characteristics of an OP – AMP loop Configuration.

(i)Output resistance "R_O" (ii) Diff. Input Resistance "R_i

2. MATERIAL REQUIRED :- OP AMP kit, connecting wire .

3. THEORY :- Differential Input resistance : - The only difference between the circuit in Figures 1-2 and 1-6 is in the way output voltage is measured. However, the input resistance seen from either input source does not depend on the way the output voltage is measured, Therefore, the input resistance R1 seen from either input source of the circuit of Figure 1-6 should be the same as that of the circuit in Figure 1-2 and is given by Equation (1-14). That is $R_{i1} = R_{i2} = 2\ \beta_{ac} r_e$

Output resistance :-

The output resistance R0 measured at collector C2 with respect to ground is equal to the collector resistor RC (see Figure 1-7(a). Thus

$R_O = R_C$

Mathematical Calculation :- (b) Differential input resistance. - Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance Ra seen from the input signal source $U_{in}1$ is determined with the signal source U_{in} 2 set at zero. Similarly, the input signal source U_{in} 1 is set at

zero to determine the input resistance R12 Seen from the input signal source U_{in} 2 See Figure 1 - 4(a). Usually, the source resistances $R_{in}1$ and $R_{in}2$ are very small and hence will be ignored in the derivation of input resistances R_{11} and R_{12} In equation form,

$$R_{i1} = \left| \frac{\upsilon_{in1}}{ib_1} \right|_{\upsilon in2=0}$$

$$= \left| \frac{\upsilon_{in1}}{i_{el}/\beta_{ac}} \right|_{Vin2=0}$$

Substituting the value of iel from Equation (1-9a), we get

$$R_{i1} = \frac{\beta_{ac} U_{in\,1}}{\dfrac{(r_e + R_E)\, U_{in\,1} - (R_E)\,(0)}{(R_e + R_E)^2 - (R_E)^2}} \qquad (1\text{-}13)$$

$$R_{i1} = \frac{\beta_{ac} (r^2_e + 2r_e R_E)}{(R_e + R_E)}$$

$$R_{i1} = \frac{\beta_{ac}\, r_e\, (r_e + 2R_E)}{(r_e + R_E)}$$

Generally, RE >> re, which implies that $(r_e + 2R_E) \cong 2R_E$ and $(r_e + R_E) \cong R_E$ therefore, Equation (1-13) can be rewritten as

$$R_{i1} = \frac{\beta_{ac}\, r_e\, (2R_E)}{(R_E)} \qquad (1\text{-}14)$$

$$R_{i1} = 2\beta_{ac}\, r_e$$

Similarly, the input resistance R_{i2} seen from the input signal source $U_{in\ 2}$ is defined as

$$R_{i2} = \left| \frac{V_{in\,2}}{i_{b2}} \right|_{vin\ 1=0}$$

$$= \frac{V_{in2}}{i_{b2} / \beta_{ac} \quad U_{in1=0}}$$

Substituting the value of i_{e2} from Equation (1-9b), we obtain

$$R_{i2} = \frac{\beta_{ac} V_{in2}}{\frac{(r_e + R_E) V_{in1} - (R_E)(0)}{(R_e + R_E)^2 - (R_E)^2}} \qquad (1\text{-}13)$$

$$R_{i2} = \frac{\beta_{ac} (r_{2e} + 2r_e R_E)}{(R_e + R_E)}$$

However, $(r_e + 2R_E) \cong 2 R_E$, and $(r_e + R_E) \cong R_E$ if $R_E >> re$. Therefore, Equation (1-15) can be rewritten as

$$R_{i2} = \frac{\beta_{ac} (r_{2e} + 2r_e R_E)}{(R_e + R_E)} \qquad (1\text{-}16)$$

$$R_{i1} = 2\beta_{ac} r_e$$

Output resistance :-

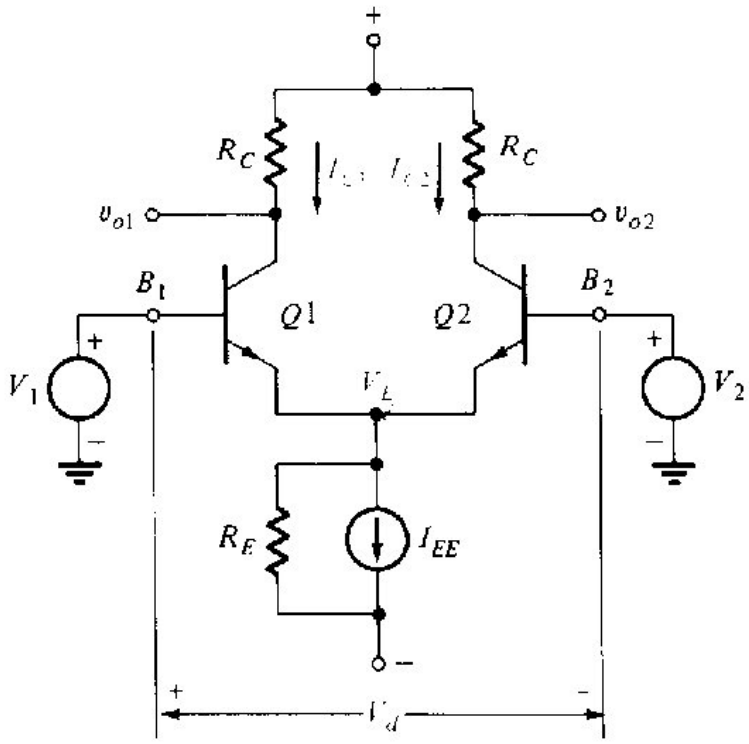
Output resistance is defined as the equivalent resistance that would be measured at either output terminal with respect to ground. Therefore, the output resistance R_{01} measured between collector C_1 and ground is equal to that of the collector resistor R_C [see Figure 1-4(a)]. Similarly, the output resistance R02 meaured at collector C_2 with respect to ground is equal to that of the collector resistor R_C. Thus

$$R_{01} = R_{02} = R_C \qquad (1\text{-}17)$$

The current gain of the differential amplifier is undefined ; therefore, the current-gain equation will not be derive for any of the four differential amplifier configurations, Furthermore, like the common-emitter amplifier, the differential amplifier is a small-signal amplifier ; therefore, it is a generally used as a voltage amplifier and not as a current or power amplifier.

4.CIRCUIT DIAGRAM :

FIGURE 2-28
The emitter-coupled or differential pair stage.



5. OBSERVATION TABLE :

SR NO	β_{ac} gain of amplifier	r_e resistance of emmiter	Input resistance $R_{i1} = 2\beta_{ac} r_e$
1			
2			

OUTPUT RESISTANCE : $R_{01} = R_{02} = R_C$

6. RESULT :-

The calculation is in according with the measured value and calculated value are equal.

7. PRECAUTION :-

1. The Kit Should be handle with care fully.
2. The wire should not be touch .
3. Take the carefully reading.

EXPERIMENT NO 2

1.OBJECTIVE :- Sturdy of Measurement of Differential Characteristics of an OP-AMP Configuration- Voltage Gain & Unity Gain Bandwidth

2.*APPARATUS* REQUIRED:- OP-AMP Kit, Trainer Connecting Wires ,Osciiloscpoe, function generator, frequency counter.

3.THEORY:- An operational amplifier (or op-amp) is a high gain amplifier which is usually powered using equal but opposite polarity voltage sources. The gain-bandwidth product (designated as GBWP, GBW, GBP or GB) for an amplifier is the product of the closed-loop gain (constant for a given amplifier) and its −3 dB bandwidth. The parameter characterizing the frequency dependence of the operational amplifier gain is the finite gain-bandwidth product (GB). As it can be seen, the amplifier takes the difference between the two input signals and amplifies it by a factor of G.

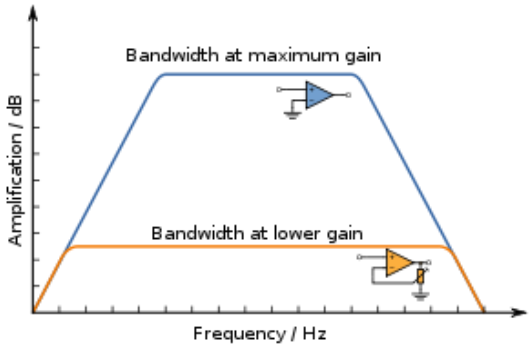
vo = G (V+ - V-) = Gvd

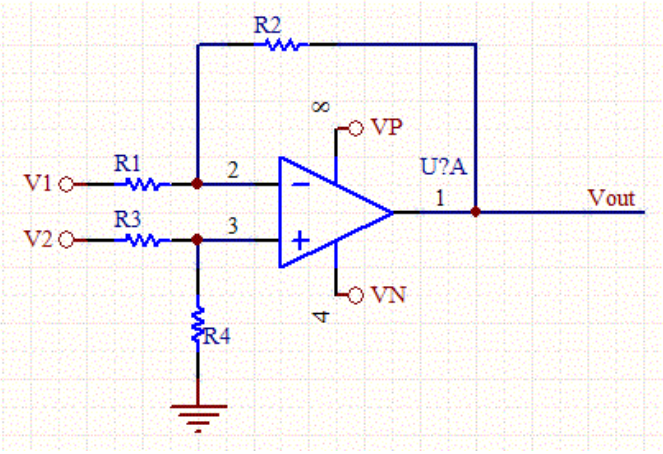
Rin represents the input impedance and Rout represents the output impedance of the amplifier. The amplifier is designed to have the following ideal characteristics:

- Input Resistance is infinite
- Output resistance is zero
- Open-loop voltage gain, G, is infinite
- Bandwidth is infinite
- vo=0 when V+ = V-

Because of these parameters, the op-amp is designed to be used in a feedback loop rather than as a stand alone (open-loop) device. This means that in a practical op-amp circuit, there is usually an external path which feeds some of the output of the op-amp back into its input. This will be investigated further in the next lab. The parameters of an actual op-amp such as the 741 differs from the ideal op-amp. . Because of these parameters, the op-amp is designed to be used in a feedback loop rather than as a stand alone (open-loop) device. This means that in a practical op-amp circuit, there is usually an external path which feeds some of the output of the op-amp back into its input. This will be investigated further in the next lab. The parameters of an actual op-amp such as the 741 differs from the ideal op-amp.

4.CIRCUIT DIAGRAM :





5.OBSERVATION TABLE :

SR NO	R_C	r_e	VOLTAGE GAIN

6. RESULT:- The calculation is in according with the measured value &calculated value are equal

7. PRECAUTIONS :

1. The Kit Should be handle with care fully.
2. The wire should not be touch .
3. Take the carefully reading.

EXPERIMENT NO 3

1.OBJECTIVE - Measurement of differential characteristics of an OP-AMP (a) Input offset voltage (b)

2.MATERIAL REQUIRED: - OP-AMP kit; Connecting wires.

3.THEORY:- Input offset voltage Vio is the differential input voltage that exists between to input terminals Of an OP-AMP without any external inputs applied. In other words ; it is the amount of the input voltage that should be applied between two input terminals in order to force the out put voltage to zero. Let as denote output offset voltage due to input offset voltage Vi0 as Voo. The output offset voltage Voo is caused by mismatching between two input terminals. Even though all the components are integrated on the same chip, it is not possible to have two transistors in the input differential amplifier stage with exactly the same characterics. This means that the collector currents in these two transistors are not equal, which causes a differential output voltage from the first stage. The output of the first stage is amplified by following stages and possibly aggravated by more mismatching in them.
Thus the output voltage caused by mismatching between two terminals is the output offset Voo. The input offset voltage can range from microvolts to millivolts and can be either polarity. Generally, bipolar op amps have lower offset voltages than JFET or CMOS types.But wait, there's more trouble. The input offset voltage will change ΔV (voltage drift) with a change in temperature ΔT. This error is a linear function of temperature and is defined by $Voff\_TC = \Delta Voff / \Delta T$ *(V/deg C)*
For an with a voltage of 25 uV / deg C, what is the drift over, say ΔT = 10 deg C?

$Voff = Voff\_TC \cdot \Delta T$

$= (25\ uV\ /\ deg\ C) \cdot 10\ deg\ C$

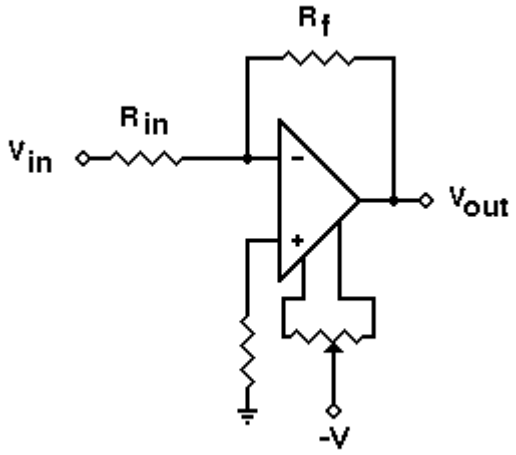
$= 0.25\ Mv$

This could add some serious error into your temperature senor circuit! But, knowing your overall error budget, you can select an op amp with a low enough offset drift to meet the target circuit performance.

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. Figure 2 shows a standard circuit for measuring offset voltage. The circuit amplifies the input offset voltage by the noise gain of 1001. The measurement is made at the amplifier output using an accurate digital voltmeter. The offset referred to the input (RTI) is calculated by dividing the output voltage by the noise gain. The small source resistance seen by the inputs results in negligible bias current contribution to the measured offset voltage. For example, 2 nA bias current flowing through the 10 Ω resistor produces a 0.02 µV error referred to the input. Many single op amps have pins available for optional offset null. To make use of this feature, two pins are joined by a potentiometer, and the wiper goes to one of the supplies through a resistor, as shown generally in Figure 4. Note that if the wiper is accidentally connected to the wrong supply, the op amp will probably be destroyed—this is a common problem, when one op amp type is replaced by another. The range of offset adjustment in a well-designed op amp is no more than two or three times the maximum VOS of the lowest grade device, in order to minimize sensitivity. Nevertheless, the voltage gain of an op amp at its offset adjustment pins may actually be greater than the gain at its signal inputs! It is therefore very important to keep these pins noise-free. Note that it is never advisable to use long leads from an op amp to a remote nulling potentiometer. Input offset

voltage (V_{os}) is the differential DC voltage required between the inputs of an amplifier, especially an operational amplifier, to make the output zero (0 volts with respect to ground, or between differential outputs if they exist, for voltage amplifiers). Typical values are around 1-10mV for cheap commercial-grade operational amplifier integrated circuits, but can be a few microvolts if nulled (assuming the IC has offset null pins for external adjustment circuits) and/or if higher quality (perhaps laser-trimmed) devices are used, although this may drift with temperature or age.Chopper amplifiers are used to reduce offset voltages.Input current (and input offset current) will affect the offset voltage unless low impedance signal sources are used; FET-input operational amplifiers tend to be better in this respect.

4.CIRCUIT DIAGRAM :



OFFSET COMPENSATING CIRCUIT

5.RESULT:-The calculation is in accordance with the measured value and calculated value is equal.

6.PRECAUTION :- (1)The circuit should be according to the diagram.
(2) The connections of the circuit should be tight.

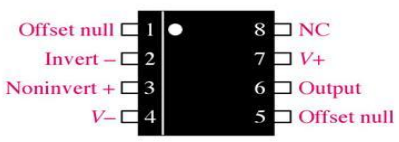
EXPERIMENT NO- 4

1.OBJECTIVE :- Offset nullification for with:(a)External biasing for inverting op-amp (b)External biasing for non-inverting op-amp

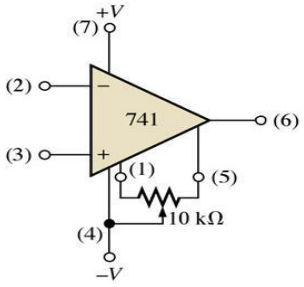
2.APPARATUS REQUIRED:- Op-amp kit, hot trainer ,connecting wire .

3.THEORY:- Offset voltage Adjustment Range :-One of the feature of the 741 family op-amp is an offset voltage null capability. The 741 op-amps have pins 1 and 5 marked as offset null for this purpose. As shown in fig 1, a 10kohms potentiometer can be connected between offset null pins 1and 5,and the wiper of the potentiometer can be connected to the negative supply –VEE.By varying the potentiometer ,the output offset voltage can be reduced to zero volts. Thus the offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying the 10kohms potentiometer .
Offset-voltage compensating network design:- The op-amp with offset –voltage compensating network is shown in fig -2 .The compensating network consist of potentiometer Ra and resistor Rb and Rc.If we are planning to make use of the op-amp as an inverting amplifier, the compensating network should be connected to the non-inverting input terminal of the op-amp.The circuit in fig 2 can be used as non inverting amplifier since the compensating network is connected to the inverting input terminal of the op-amp .

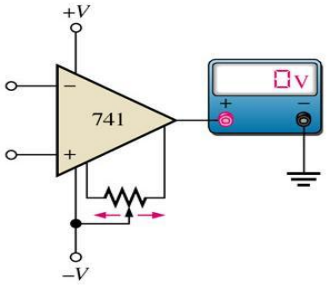
4.CIRCUIT DIAGRAM :-



(a) 8-pin DIP or SMT package



(b) External potentiometer



(c) Adjust for zero output

5.RESULT : This is generally done by connecting an external potentiometer to pins Designated with *Offset Null*. With zero input voltage, the output is set to zero by adjusting the potentiometer.

6.PRECAUTIONS :

(1)Op-amp kit should be handle with care.
(2)Wire should be connected properly.

EXPERIMENT NO 5

1.OBJECTIVE :- Inverting amplifier (a) AC Analysis (b)DC Analysis (c)Unity Gain

2.MATERIAL REQUIRED:- Op-amp kits, connecting wire, trainer.

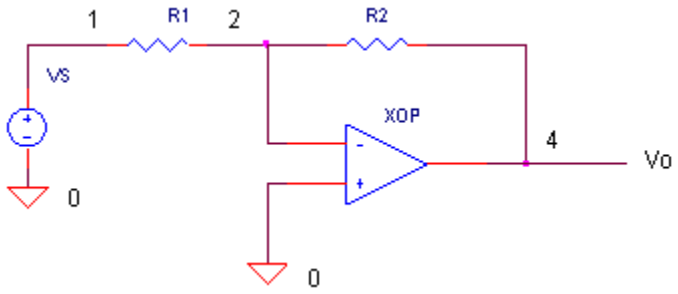
3.THEORY:- DC Amplifier – Basically, an op-amp can amplifier two types of signals: dc and ac. In a dc amplifier the output signal changes in response to change in its dc input levels. A dc amplifier can be inverting, non inverting, or differential, as shown in figure. To reduce the output offset voltage to zero, that is, to input the accuracy of the dc amplifier the offset null circuitry of the op-amp should be used. For op-amp without offset null capability, the external offset voltage compensating network should be used.

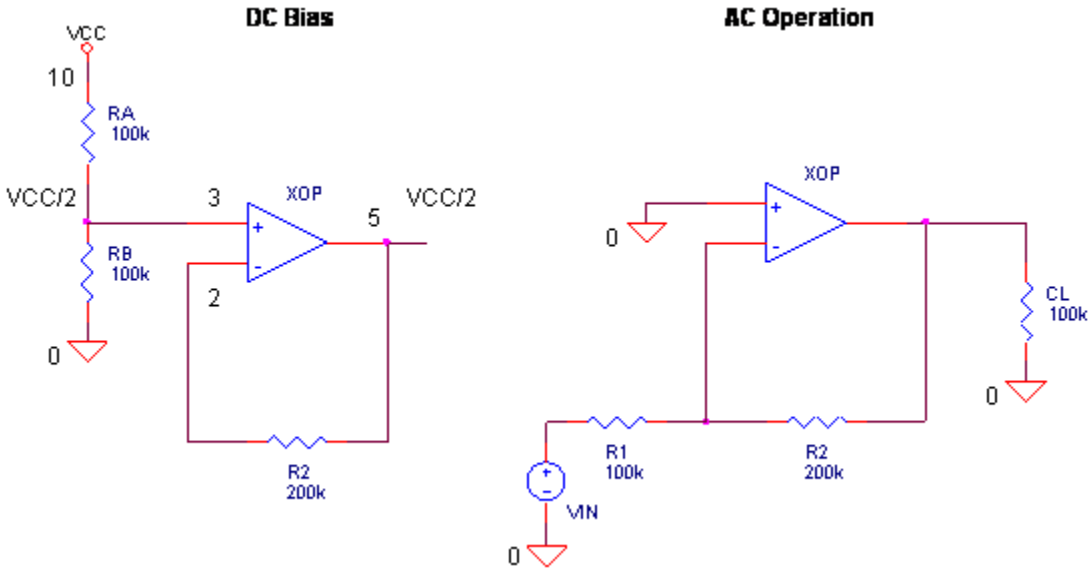
AC Amplifier:- However if the designer needs the ac response characteristic the op-amp, that is, low and high frequency limits, or if the ac input is reading on some dc level, it is necessary to use an ac amplifier with a coupling capacitor.

Unity gain:- If we need an output signal equal in amplitude but opposite in phase to that of the input signal, we can use the inverter. The inverting amplifier work as an inverter if $R_1 = R_F$ Since the inverter is a special case of the inverting amplifier, all the equation develop for the inverting amplifier are also applicable here. The equation can be applied by merely substituting (A/2) for (1+ AB), since B = ½.

Amplifier DC performance is affected by a variety of Op Amp characteristics. Not all of these factors are commonly well understood. This analysis will develop complete expressions for analyzing the DC performance of an differential amplifier including the effect of bias current, offset current and offset voltage. Accurate assessment of performance over a wide range of conditions will then be possible. The two amplifier input terminal currents will be labeled I_{minus} and I_{plus} . Most bipolar Op Amps (but not all) have input stages arranged such that current flows into the amplifier input pins. The situation is more complex with FET input devices where the dominant input current term is a leakage current.

4.CIRCUIT DIAGRAM:-





5.RESULT:- The calculation is in according with the measured value and calculated value are equal.

6.PRECAUTION:- 1. The kit should be handle with carefully.
2. The wire should not be touched.
3. Take the carefully reading.

EXPERIMENT NO 6

1.OBJECT:- Non Inverting amplifier (a) AC Analysis (b)DC Analysis (c)Unity Gain Buffer

2.MATERIAL REQUIRED:- Op-amp kits, connecting wire, trainer.

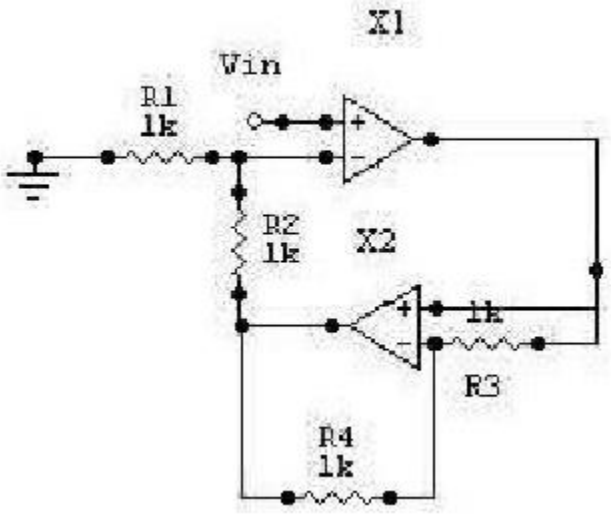
3.THEORY:- DC Amplifier – Basically, an op-amp can amplifier two types of signals: dc and ac. In a dc amplifier the output signal changes in response to change in its dc input levels. A dc amplifier can be inverting, non inverting, or differential, as shown in figure. To reduce the output offset voltage to zero, that is, to input the accuracy of the dc amplifier the offset null circuitry of the op-amp should be used. For op-amp without offset null capability, the external offset voltage compensating network should be used.

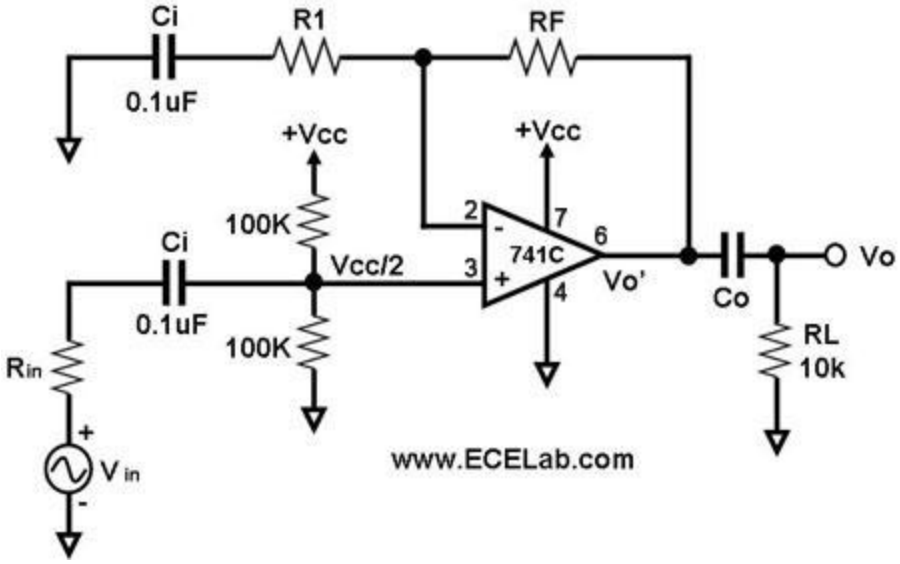
AC Amplifier:- However if the designer needs the ac response characteristic the op-amp, that is, low and high frequency limits, or if the ac input is reading on some dc level, it is necessary to use an ac amplifier with a coupling capacitor.

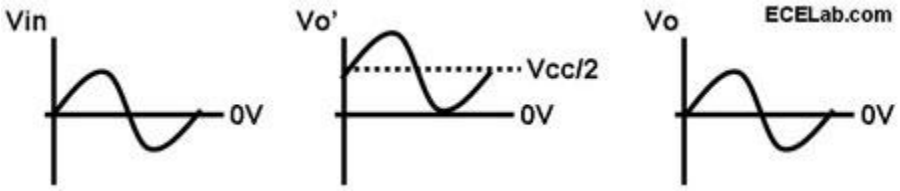
Unity gain buffer:- The lowest gain that can be obtained from a noninverting amplifier with feedback is 1. When the noninverting amplifier is configured for unity gain, it is called a voltage follower because the output voltage is equal to and in phase with the input. In other words, in the voltage follower the output followers the input.
This is a circuit for amplifying an AC input voltage with no inversion at the output. The active component of this circuit is an operational amplifier, which is configured as a non-inverting amplifier. To ensure that the output can swing in the positive and negative directions equally, a DC voltage equal to Vcc/2 is inserted at the non-inverting input through the voltage divider formed by the 100K resistors.

When Vin is an AC signal within the circuit's bandwidth, the gain G of the amplifier is determined by RF and R1, i.e., G = 1 + RF/R1. The op amp output Vo' is the sum of the DC (Vcc/2) and AC output voltages. Output capacitor Co removes the DC component of Vo', causing the final output Vo of the circuit to be a purely AC amplified copy of the input waveform, or Vo = (1 + RF/R1) Vin.
graphically shows an example of how an AC input voltage is amplified by the AC amplifier shown in Figure 1. The op amp's output, Vo', is an amplified copy of the input voltage, shifted upwards by a DC component equal to Vcc/2. The final output Vo of the circuit is a purely AC amplified copy of the input waveform, since the DC component has already been removed by Co.

4.CIRCUIT DIAGRAM:-


X1
Vin
R1
1k
R2
1k
X2
1k
R3
R4
1k


Ci
0.1uF
R1
RF
+Vcc
+Vcc
100K
Ci
0.1uF
Vcc/2
100K
2
7
6
741C
3
4
Vo'
Co
Vo
Rin
RL
10k
Vin
www.ECELab.com


Vin
0V
Vo'
Vcc/2
0V
Vo
ECELab.com
0V

5.RESULT:- The calculation is in according with the measured value and calculated value are equal.

6.PRECAUTION:- 1. The kit should be handle with carefully.
2. The wire should not be touched.
3. Take the carefully reading.

EXPERIMENT NO 7

1.OBJECTIVE : OP AMP as (a) adder (b)substractor

2.MATERIAL REQUIRED : OP AMP kit, connecting wire

3.THEORY : (a) If we take three equal resistors and connect one end of each to a common point, then apply three input voltages (one to each of the resistors' free ends), the voltage seen at the common point will be the mathematical *average* of the three. his circuit is commonly known as a *passive averager*, because it generates an average voltage with non-amplifying components. *Passive* simply means that it is an unamplified circuit. The large equation to the right of the averager circuit comes from Millman's Theorem, which describes the voltage produced by multiple voltage sources connected together through individual resistances. Since the three resistors in the averager circuit are equal to each other, we can simplify Millman's formula by writing R_1, R_2, and R_3 simply as R (one, equal resistance instead of three individual resistances):

$$V_{out} = \frac{\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}}{\frac{1}{R} + \frac{1}{R} + \frac{1}{R}}$$

$$V_{out} = \frac{\frac{V_1 + V_2 + V_3}{R}}{\frac{3}{R}}$$

$$V_{out} = \frac{V_1 + V_2 + V_3}{3}$$

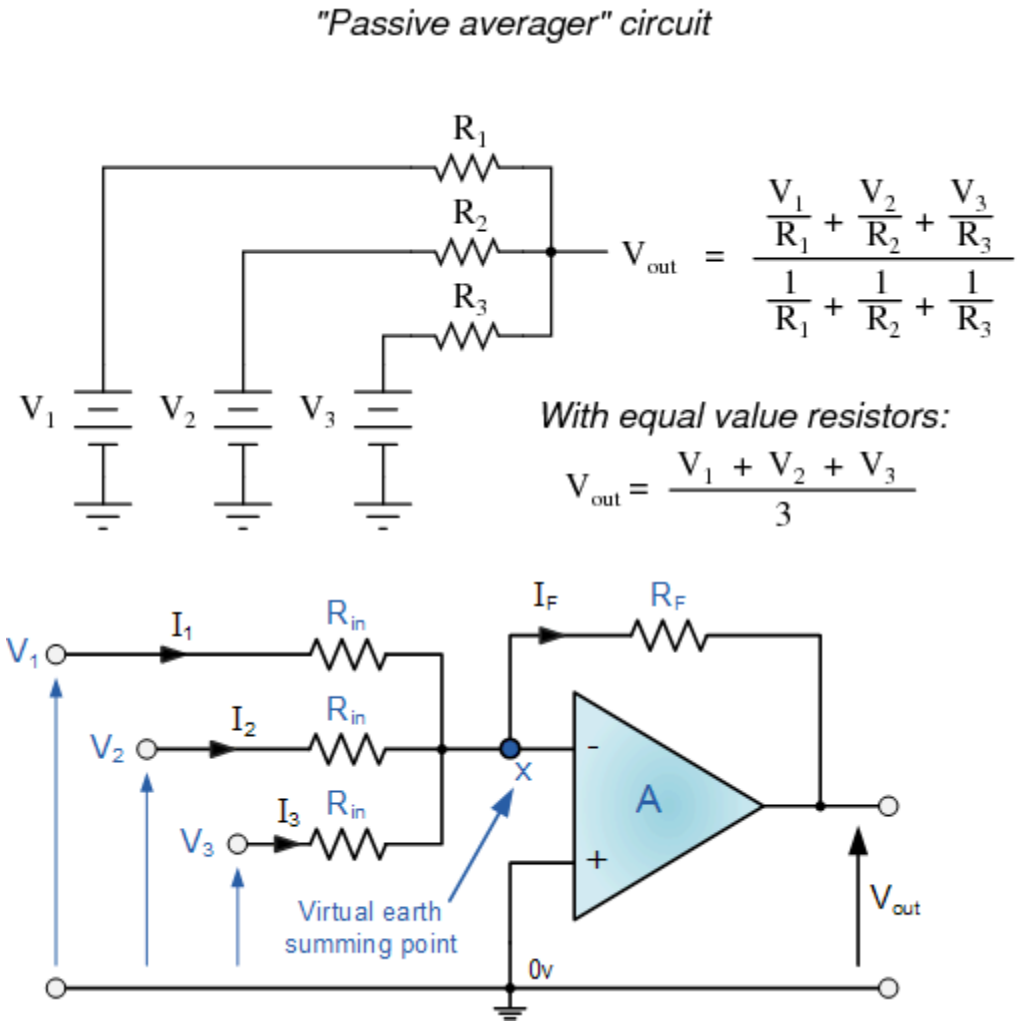
$$V_{out} = 3 \frac{V_1 + V_2 + V_3}{3}$$

$$V_{out} = V_1 + V_2 + V_3$$

(B) Basically, as we saw in the first tutorial about operational amplifiers, all op-amps are "Differential Amplifiers" due to their input configuration. But by connecting one voltage signal onto one input terminal and another voltage signal onto the other input terminal the resultant output voltage will be proportional to

the "Difference" between the two input voltage signals of V1 and V2. Then differential amplifiers amplify the difference between two voltages making this type of circuit a Subtractor unlike a summing amplifier which adds or sums together the input voltages. This type of operational amplifier circuit is commonly known as a **Differential Amplifier** configuration

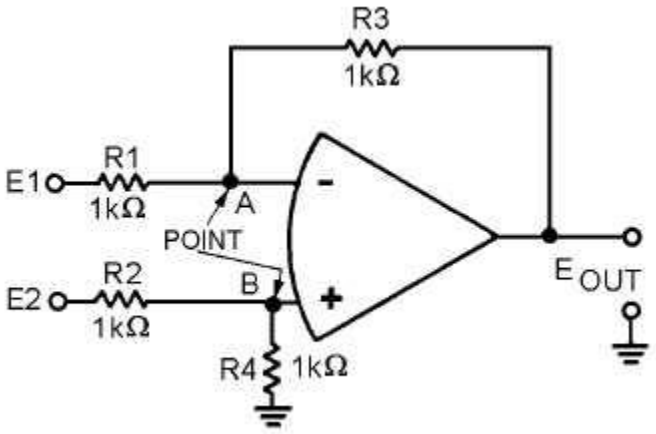
4.CIRCUIT DIAGRAM :



$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$



$E_{out} = E2 - E1$

RESULT : The output of op amp as adder and substractor is studied.

PRECAUTIONS :

1. The Kit Should be handle with care fully.
2. The wire should not be touch .
3. Take the carefully reading.

EXPERIMENT NO 8

1.OBJECTIVE : OP-AMP (A) as integrator.(B) differentiator (c) inverter (d)buffer

2.APPARATUS REQUIRED :OP-AMP kit, connector wire .

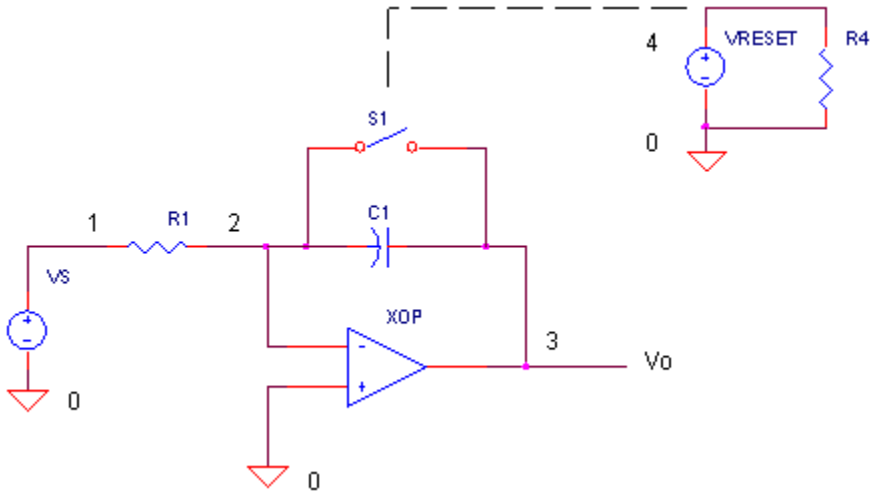
3.THEORY : (a)The integrator basically works like this: whatever current I you get flowing in R1, gets integrated across capacitor C1. The output voltage Vo is simply the voltage across C1. One great application of the integrator is generating a ramp voltage. You can do this by placing a fixed voltage at VS that forces a constant current through R1. The capacitor then integrates this current creating a ramping voltage. The action is just like a garden hose running water at a constant rate causing the level in a bucket to rise steadily. The smaller the diameter bucket (smaller capacitor), the faster the increase in water level (greater voltage). The switch is needed to discharge the capacitor (empty the bucket) at the end of a ramping cycle.

(b)Its number one function: c*reate an output voltage proportional to the rate of change of the input voltage*. This leads to cool applications such as extracting edges from square waves, converting sinewaves into cosines and changing triangle waves into square waves. But most circuits are susceptible to some trouble and this one's vulnerabilities are *instability and noise*. However, remedies are available to reduce the troubles without losing the desired function.
(c) An input voltage, V_{in} is applied to the input resistor, R_{in}. The amplifier, represented by the triangle, amplifies the input voltage it receives and inverts its polarity, producing an output voltage, V_{out}. This same output voltage is also applied to a feedback resistor, R_f, which is connected to the amplifier input along with R_{in}.The amplifier itself has a very high voltage gain. As a result, the junction of the two resistors, which is also the amplifier input, must be virtually at ground potential. A non-zero input voltage will be amplified so much that the output voltage would try to exceed its electronic limits. At the same time, the amplifier requires almost zero input current to operate. Therefore, the input current (V_{in}/R_{in}) must be the same as the feedback current (V_{out}/R_f). This in turn means that the effective gain of the circuit with feedback in place is simply the resistance ratio, R_f/R_{in}. This is the beauty and value of the operational amplifier: we can obtain precision results if we use precision resistors.

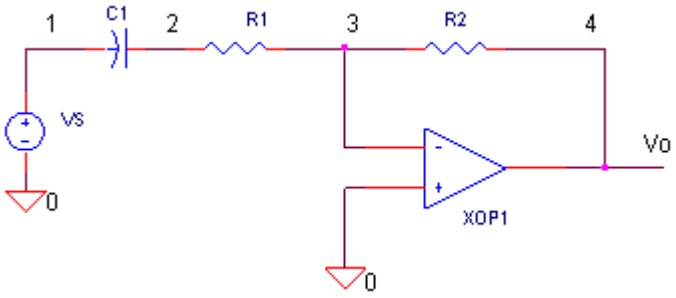
If $R_f = R_{in}$, $V_{out} = -V_{in}$.

(d) op amp as buffer If the voltage is transferred unchanged (the voltage gain A_v is 1), the amplifier is a unity gain buffer; also known as a voltage follower because the output voltage *follows* or tracks the input voltage. Although the voltage gain of a voltage buffer amplifier may be (approximately) unity, it usually provides considerable current gain and thus power gain. However, it is commonplace to say that it has a gain of 1 (or the equivalent 0 dB), referring to the voltage gain.

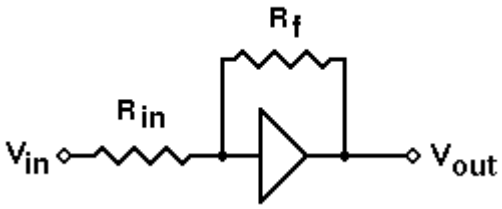
4.CIRCUIT DIAGRAM :



$$Vo = -\frac{1}{C1}\int_0^T \frac{Vs}{R1}\,dt$$

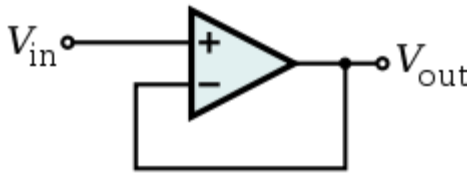


$Vo = - C1 \cdot R2 \cdot dVS / dt$



Op amp as inveter

If $R_f = R_{in}$, $V_{out} = -V_{in}$.



An op-amp–based unity gain buffer amplifier

5.RESULT : The operation of op amp as integrator, differentiator, buffer and inverter is studied.

6.PRECAUTIONS :- (1) Avoid loose connection.

(2) Before on the switch of the trainer kit be sure that the connecting wires are connected correctly as per experiment.

EXPERIMENT NO 9

1.OBJECTIVE : - op-amp(operational-amplifier) an active filter. Low pass filter
High pass filter
Band pass filter

2.MATERIAL REQUIRED – op- amp kit, connecting weirs.

3.THEORY : – An electric filter is often a frequency – selective circuit that passes a specified band of frequencies and blocks are attenuates singles of frequencies outside this band.
Filters may be classified in a number of ways: analog or digital , passive or active ,audio (AF) or radio frequency (RF)

inductors are often not used because they are very large, costly and may dissipate more power. Inductors also emit magnetic fields.

Although active filters are most extensively used in the fields of communication and single processing, they are employed in one form or another in almost all sophisticated electronic systems. Radio, television, telephone, radar, space, satellites and biomedical equipments are but a few systems that employ active filters.

The most commonly used filters are these: Low – pass filter ,High - pass filter,Band - pass filter,Band – reject filter,All – pass filter.

The basic first-order high-pass filters use the same components as the low-pass filters we just studied. However, their positions are swapped. Thus, the RC high-pass filter has the capacitor in series with the signal and the resistor across the output, as shown in the first diagram to the right. At high frequencies, C has very low impedance, and the signal passes through unhindered. As the frequency decreases, however, X_C becomes significant, until at the cutoff frequency, $X_C = R$, just as with the low-pass filter. At still lower frequencies, X_C increases, and less of the signal reaches the output. A low-pass filter is a filter that passes low-frequency signals but attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. It is sometimes called a high-cut filter, ortreble cut filter when used in audio applications. A low-pass filter is the opposite of a high-pass filter, and a band-pass filter is a combination of a low-pass and a high-pass.

Low-pass filters exist in many different forms, including electronic circuits (such as a hiss filter used in audio), digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. The moving average operation used in fields such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the longer-term trend.

One useful feature of the RC high-pass filter is that the capacitor serves to block direct current between v_{IN} and v_{OUT}. Thus, two circuits that operate at different DC voltages can be connected by this type of high-pass filter without encountering any problems with dc component bias voltages as a consequence.

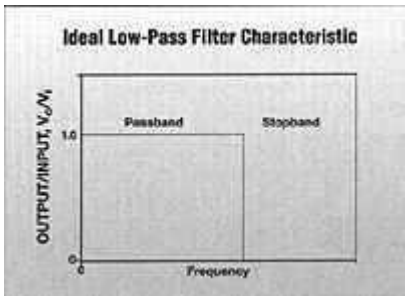
band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range. An example of an analogueelectronic band-pass filter is an RLC circuit (a resistor–inductor–capacitor circuit). These filters can also be created by combining a low-pass filter with a high-pass filter.

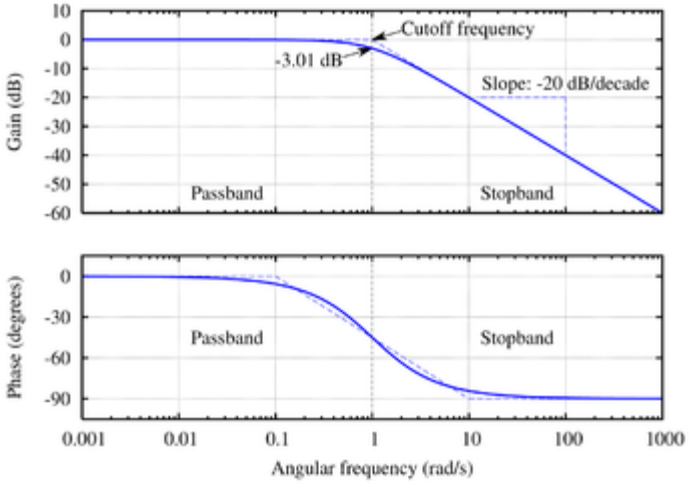
Bandpass is an adjective that describes a type of filter or filtering process; it is frequently confused with passband, which refers to the actual portion of affected spectrum. The two words are both compound words that follow the English rules of formation: the primary meaning is the latter part of the compound, while the modifier is the first part. Hence, one may correctly say 'A dual bandpass filter has two passbands'. A bandpass signal is a signal containing a band of frequencies away from zero frequency, such as a signal that comes out of a bandpass filter.[2]

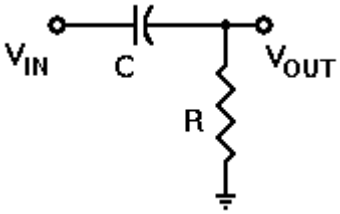
. The ideal response is shown by dashed curves, will the solid lines indicate the practical filter response. A low – pass filter has a constant gain from 0 Hz to a high cut of frequency fH. Therefore, the bandwidth is also fH. At fH the gain is down by 3 dB, after that (f >fH) is decreases with the increase in output frequency. The frequencies between 0 Hz and fH are known as the passband frequencies, whereas the range of frequencies, those beyond fH , that are attenuated includes the stop band frequencies.

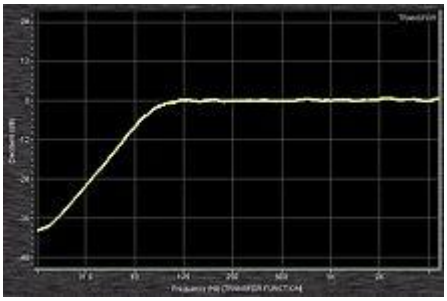
figure (b) shows a high – pass filter with a stop band 0 < f < fL and a pass band f > fL. fL is the low cutoff frequency, and f is the operating frequency .A band – pass filter has a passband between two cutoff frequencies fH and fL, where fH> fL , and two stopbands, 0 < f < fL and f> fH. The bandwidth of the band pass filter, therefore, is equal to fH - fL .

4.CIRCUIT DIAGRAM :

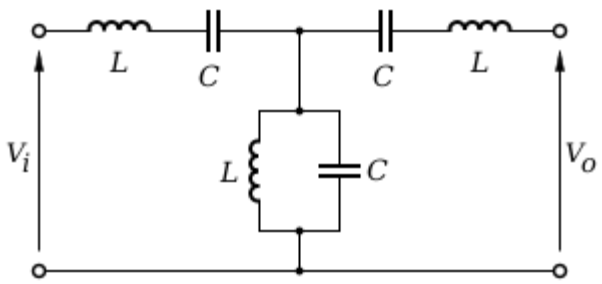




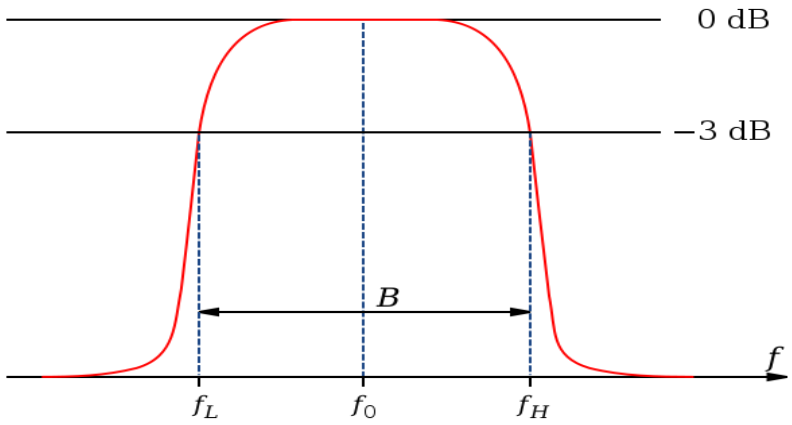




75 Hz "low cut" filter from an input channel of a Mackie 1402 mixing console as measured by Smaart software. This high-pass filter has a slope of 18 dB per octave.



A medium-complexity example of a band-Pass filter



Bandwidth measured at half-power points (gain -3 dB, √2/2, or about 0.707 relative to peak) on a diagram showing magnitude transfer function versus frequency for a band-pass filter

5.RESULT – The characteristics shows the variation of gain with frequency of the filter.

6.PRECAUTIONS: -

1. The Kit Should be handle with care fully.
2. The wire should not be touch .
3. Take the carefully reading.

EXPERIMENT NO 10

1.OBJECTIVE :-Wave shaping: Astable multivibrator using OP-AMP.(a)Astable multivibrator Timer ICand op amp (b) Monostable multivibrator using Timer IC.

2.MATERIAL REQUIRED : Astable multivibrator and monostable multivibrator.

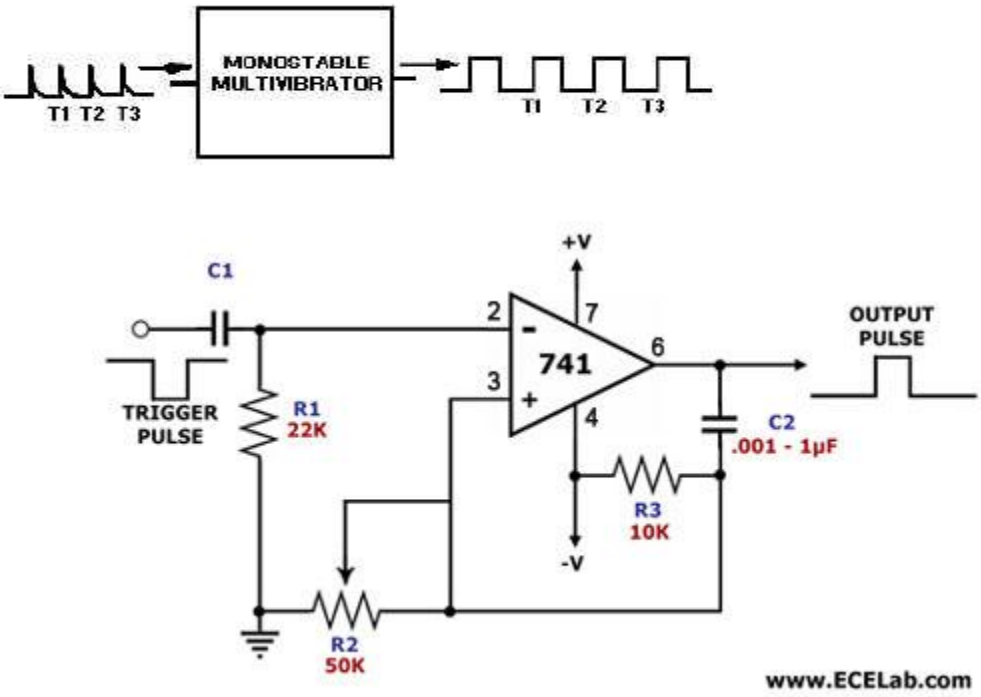
3.THEORY:- Each time the input signal crosses zero in the negative direction the output of the comparator goes low. Three microseconds later the Cref charge/discharge control circuit is enabled, which instantaneously connects the reference capacitor Cref to the reference voltage Vref. This action charges Cint each time with a precise amount of voltage until the voltage across it can no longer increase. The charging path is through the output terminal of the op-amp, through Cint, through Cref,and finally through Vref . On the other hand, each time the input waveform crosses zero in the positive direction, the output of the comparator switches high. This disable the Cref charge/discharge control circuit , and Cref is shorted out. However ,the voltage across Cint is retained because the only discharge path for Cint is through Rint , which is very large (1Mohms). The voltage across Cintis the output voltage Vo.

The amount of ripple on Vo is inversely proportional to Cint and the frequency of the input Fin. This means that for low frequencies Cint can be increased in the range from 1 to 100microf to reduce the ripple. To eliminate the ripple on Vo, an extra op-amp that is operating in the common mode configuration shown in Fig 1 can be connected to the output of the F/V converter of Fig 2 . Because of the common mode configuration, the ac ripple is canceled at the output of an op-amp provided that both(+) and (-) inputs have the same equal. Besides that, the circuit in Fig 1 has a dc gain of unity, so output voltage is equal to input.

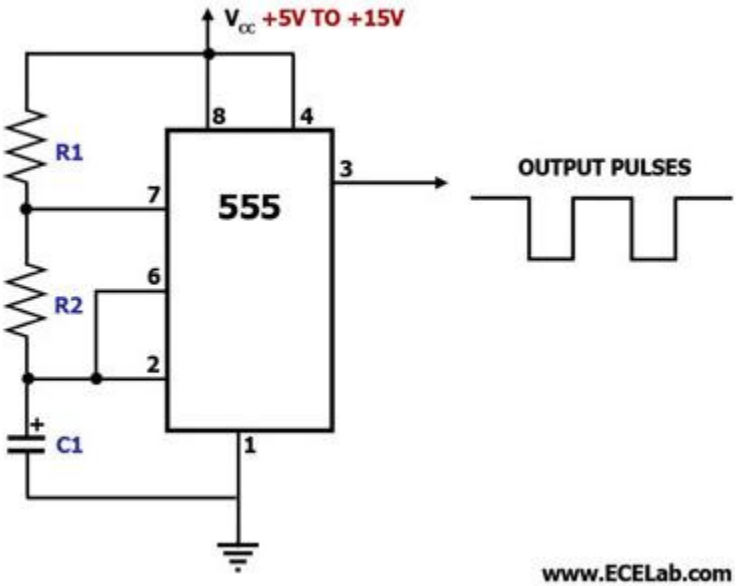
In the F/V converter of Fig 2, outputs Fo and Fo/ 2 are optional because these output are useful in only some application. The output Fo follows in the input frequency wave form with a 3-microsecond delay on the rising edge . Fo/2 is a square wave with a frequency one-half of Fo. If Fo and Fo/2 output are not used ,pins 8and 10 may be connected to ground.

Although the F/V converter accepts any input wave shape, the circuit will work only if the positive pulse width of the input wave form is at least 5microsecond and the negative pulse width is >- o.5 microsecond. When Fin max is less than 1KHZ, the duty cycle should be greater than 20% to ensure that Cref is fully charged and discharged . This is a monostable multivibrator circuit that employs a single op amp. The main component of this circuit is the 741, a general-purpose operational amplifier. A monostable multivibrator is a timing circuit that changes state once triggered, but returns to its original state after a certain time delay. It got its name from the fact that only one of its output states is stable. It is also known as a 'one-shot'.
A negative trigger pulse at the input forces the output of the op amp to logic 'high'. This charges up C2 which keeps the non-inverting input of the op amp temporarily higher than the inverting input, maintaining the output high for a certain period of time. Eventually C2 discharges to ground and the op amp output swings back to logic 'low'. The duration of the pulse is defined by R2 and C2. The 'one-shot' has several applications, which include dividing the frequency of the input signal and converting an irregular input pulse to a uniform output pulse.

4.CIRCUIT DIAGRAM:-



Op-Amp Monostable Multivibrator Circuit Diagram



ASTABLE MULTIVIBRATOR USING IC 555

5.RESULT:-The operation of astable and monostable multivibrator is studied.

6.PRECAUTION:- (1) Op-amp kit is handle with care.
(2) wire should be connected properly.

EXPERIMENT NO 11

1.OBJECTIVE : Signal generator using op amp (a) triangular wave generator.

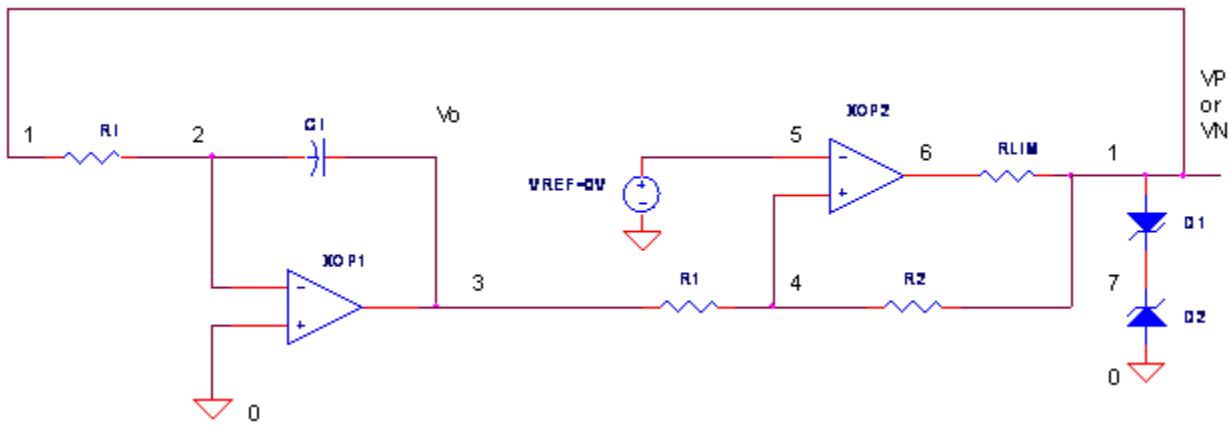
2.MATERIAL REQUIRED : triangular wave generator.

3.THEORY : Ramp Up Connect RI to VN and what happens? With V- held at the virtual

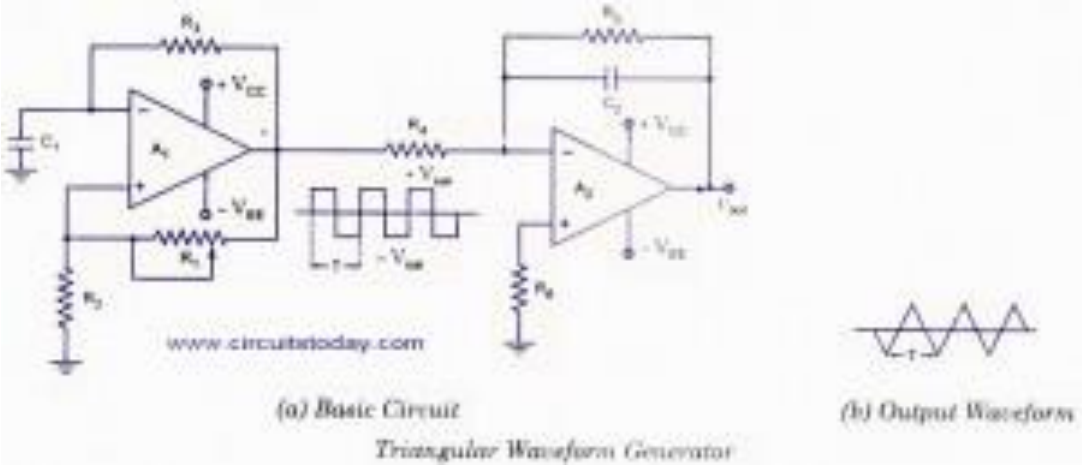
ground (0V), a constant current flows from V- to VN. Iin = VN / RI.
CI integrates Iin creating a positive linear ramp at Vo. The ramp is linear because Vo changes proportionally to the time elapsed ΔT. ΔVo = - VN / (CI · RI) · ΔTRamp Down Connect RI to VP and a constant current flows from VP to V-, Iin = - VP / RI. Now Vo ramps down linearly ΔVo = - VP / (CI · RI) · ΔT
The op-amp triangular-wave generator is another example of a relaxation oscillator. We know that the integrator output waveform will be triangular if the input to it is a square-wave. It means that a triangular-wave generator can be formed by simply cascading an integrator and a square-wave generator, as illustrated in figure. This circuit needs a dual op-amp, two capacitors, and at least five resistors. The rectangular-wave output of the square-wave generator drives the integrator which produces a triangular output waveform. The rectangular-wave swings between $+V_{sat}$ and $-V_{sat}$ with a time period determined from equation. The triangular-waveform has the same period and frequency as the square-waveform. Peak to-peak value of output triangular-waveform can be obtained from the following equation.

The input of integrator A_2 is a square wave and its output is a triangular waveform, the output of integrator will be triangular wave only when $R_4 C_2 > T/2$ where T is the (period of square wave. As a general rule, R_4C_2 should be equal to T. It may also be necessary to shunt the capacitor C_2 with resistance $R_5 = 10 R_4$ and connect an offset volt compensating network at the non-inverting (+) input terminal of op-amp A_2 so as to obtain a stable triangular wave. Since the frequency of the triangular-wave generator like any other oscillator, is limited by the op-amp slew-rate, a high slew rate op-amp, like LM 301, should be used for the generation of relatively higher frequency waveforms.

4.CIRCUIT DIAGRAM :



triangular wave generator



5.RESULT : The operation of triangular wave generator is studied.

6.PRECAUTIONS : 1.Connections should be tight.

2.power supply should be switched on after checking the circuit.

EXPERIMENT NO 12

1.OBJECTIVE :- Schmitt Trigger OP-AMP / Timer IC Saw tooth wave generator Ramp generator

2.MATERIAL REQUIRED : Saw tooth wave generator Ramp generator

3.THEORY- A Schmitt trigger circuit is a fast-operating voltage-level detector. When the input voltage arrives at the upper or lower trigger levels, the output changes rapidly. The circuit operates with almost any type of input waveform, and it gives a pulse-type output.

The circuit of an op-amp Schmitt trigger circuit is shown in figure. The input voltage v_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means the circuit uses positive voltage feedback instead of negative feedback, that is, in this circuit feedback voltage aids the input voltage rather than opposing it. For instance, assume the inverting input voltage to be slightly positive. This will produce a negative output voltage. The voltage divider feedsback a negative voltage to the non-inverting input, which results in a larger negative voltage. This feedsback more negative voltage until the circuit is driven into negative saturation. If the input voltage were, slightly negative instead of positive, the circuit would be driven into the positive saturation. This is the reason the circuit is also referred to as regenerative comparator.

When the circuit is positively saturated, a positive voltage is fedback to the non-inverting input. This positive input holds the output in the high state. Similarly, when the output voltage is negatively saturated, anegative voltage is fedback to the non-inverting input, holding the output in the low state. In either case, the positive feedback reinforces the existing output state.

The feedback fraction, $\beta = R_2/R_1 + R_2$ When the output is positively saturated, the reference voltage applied to the non-inverting input is $V_{ref} = + \beta V_{sat}$ When the output is negatively saturated, the reference voltage is $V_{ref} = - \beta V_{sat}$

The output voltage will remain in a given state until the input voltage exceeds the reference voltage for that state. For instance, if the output is positively saturated, the reference voltage is $+ \beta V_{sat}$. The input voltage v_{in} must be increased slightly above $+ \beta V_{sat}$ to switch the output voltage from positive to negative, as shown in figure. Once the output is in the negative state, it will remain there indefinitely until the input voltage becomes more negative than $-\beta V_{sat}$. Then the output switches from negative to positive. This can be explained from the input-output characteristics of the Schmitt trigger shown in figure, as below.

Schmitt Trigger A Schmitt trigger circuit is a fast-operating voltage-level detector. When the input voltage arrives at the upper or lower trigger levels, the output changes rapidly. The circuit operates with almost any type of input waveform, and it gives a pulse-type output.

The circuit of an op-amp Schmitt trigger circuit is shown in figure. The input voltage v_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means the circuit uses positive voltage feedback instead of negative feedback, that is, in this circuit feedback voltage aids the input voltage rather than opposing it. For instance, assume the inverting input voltage to be slightly positive. This will produce a negative output voltage. The voltage divider feedsback a negative voltage to the non-inverting input, which results in a larger negative voltage. This feedsback more negative voltage until the circuit is driven into negative saturation. If the input voltage were, slightly negative instead of positive, the circuit would be driven into the positive saturation. This is the reason the circuit is also referred to as regenerative comparator.

When the circuit is positively saturated, a positive voltage is fedback to the non-inverting input. This positive input holds the output in the high state. Similarly, when the output voltage is negatively saturated, a negative voltage is feedback to the non-inverting input, holding the output in the low state. In either case, the positive feedback reinforces the existing output state. The feedback fraction, $\beta = R_2/R_1 + R_2$

When the output is positively saturated, the reference voltage applied to the non-inverting input is $V_{ref} = + \beta V_{sat}$ When the output is negatively saturated, the reference voltage is $V_{ref} = - \beta V_{sat}$

The output voltage will remain in a given state until the input voltage exceeds the reference voltage for that state. For instance, if the output is positively saturated, the reference voltage is $+ \beta V_{sat}$. The input voltage v_{in} must be increased slightly above $+ \beta V_{sat}$ to switch the output voltage from positive to negative, as shown in figure. Once the output is in the negative state, it will remain there indefinitely until the input voltage becomes more negative than $-\beta V_{sat}$. Then the output switches from negative to positive. This can be explained from the input-output characteristics of the Schmitt trigger shown in figure, as below.Characteristics of the Schmitt trigger

Assume that input voltage v_{in} is greater than the $+ \beta V_{sat}$, and output voltage v_{OUT} is at its negative extreme (point 1). The voltage across R_2 in the figure is a negative quantity.

As a result, v_{in} must be reduced to this negative voltage level (point 2 on the characteristics) before the output switches positively (point 3). If the input voltage is made more negative than the $- \beta V_{sat}$, the output remains at $+ +v_{OUT}$ (points 3 to 4). For the output to go negative once again, v_{in} must be increased to the $+ \beta V_{sat}$ level (point 5 on the characteristics).

In figure, the trip points are defined as the two input voltages where the output changes states. The upper trip point (abbreviated UTP) has a value

$UTP = \beta V_{sat}$ and the lower trip point has a value

$LTP = - \beta V_{sat}$

The difference between the trip points is the hysteresis H and is given as

$H = + \beta V_{sat} - (-\beta V_{sat}) = 2 \beta V_{sat}$

The hysteresis is caused due to positive feedback. If there were no positive feedback, β would equal zero and the hysteresis would disappear, because the trip points would both equal zero.

Hysteresis is desirable in a Schmitt trigger because it prevents noise form causing false triggering.

To design a Schmitt trigger, potential divider current I_2 is once again selected to be very much larger than the op-amp input bias current. Then the resistor R_2 is calculated from equation

$R_2 = UTP/I_2$

and R_1 is determined from

$R_{1\,=}\,(V_{OUT} - UTP) / I_2$

Saw tooth wave generator.

The difference between the triangular and sawtooth waveforms is that in triangular waves the rise time is always equal to its fall time while the sawtooth waveforms have different rise and fall times i.e. sawtooth wave may rise positively many times faster than it falls negatively or vice-versa.

The circuit shown in figure provides the ability of controlling ramp generation with an external signal. In the circuit shown, an NPN BJT has been placed around the charging capacitor C and emitter of the transistor is tied to the inverting (-) terminal of the op-amp, which is at virtual ground. Resistor R_B is for limiting the base current and so for protecting the BJT. However, R_B is to be kept relatively small to assure that the transistor can be driven into saturation. The part of the circuit consisting of the capacitor C, transistor,zener diode and the resistors form a constant current source to charge the capacitor. Initially assume the capacitor is fully discharged. The voltage across it is zero and hence the internal comparators inside the 555 connected to pin 2 causes the 555's output to go high and the internal transistor of 555 shorting the capacitor C to ground opens and the capacitor starts charging to the supply voltage. As it The frequency of the circuit is given by:

f = (Vcc-2.7)/(R*C*Vpp) charges, when its voltage increases above 2/3rd the supply voltage, the 555's output goes low, and shorts the C to ground, thus discharging it. Again the 555's output goes high when the voltage across C decreases below 1/3rd supply. Hence the capacitor charges and discharges between 2/3rd and 1/3rd supply.

Note that the output is taken across the capacitor. The 1N4001 diode makes the voltage across the capacitor go to ground level (almost).

where: Vcc= Supply voltage.

Vpp= Peak to peak voltage of the output required.

Choose proper R,C,Vpp and Vcc values to get the required 'f' value.

the capacitor is slowly charged through resistor R and finally after reaching the base-emitter voltage of PNP transistor, the PNP transistor begin conducting and activate the NPN transistor. The activation of NPN transistor is positively fed back to the PNP transistor so the transistors short the capacitor C to ground,

discharging its voltage until zero in very fast manner. After the capacitor voltage falls down to zero,

RAMP GENERATOR

Sometimes it is felt necessary to provide a relatively slow linear ramp with a rapid fall (or rise in the case of a negative ramp) at its end. This is a sawtooth wave. Also, in applications such as time base generators and power control circuits, the sawtooth must be triggered by (or be synchronized with) some control signal.The difference between the triangular and sawtooth waveforms is that in triangular waves the rise time is always equal to its fall time while the sawtooth waveforms have different rise and fall times i.e. sawtooth wave may rise positively many times faster than it falls negatively or vice-versa.

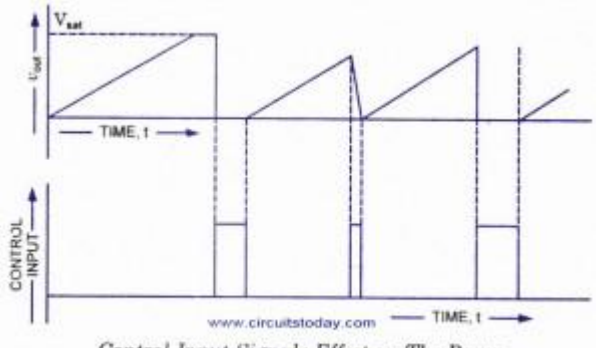
The circuit shown in figure provides the ability of controlling ramp generation with an external signal. In the circuit shown, an NPN BJT has been placed around the charging capacitor C and emitter of the transistor is tied to the inverting (-) terminal of the op-amp, which is at virtual ground. Resistor R_B is for limiting the base current and so for protecting the BJT. However, R_B is to be kept relatively small to assure that the transistor can be driven into saturation.

With a zero or negative control input voltage, the transistor is off. The capacitor charges up from the op-amp output, through *C, R_{in} and to V-. The charge rate is given as*

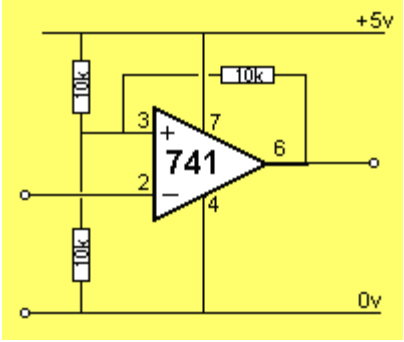
Rate = V- / R_{in} *C If the control voltage is not changed, the capacitor C *will eventually charge up, and hold the output at + V_{sat}.* However, when a positive control input is applied, the transistor gets turned on. If this voltage is large enough to force transistor into saturation the capacitor is effectively short-circuited. The capacitor C rapidly discharges.

The output voltage falls to zero (actually about 0.2 V) and stays there as long as positive control voltage keeps the transistor saturated. The expected obtainable waveform is given in figure. For control of negative going ramps, the circuit shown in figure will require several minor changes. First, the charging voltage, connected to R_{in}, polarity will have to be reversed to V+. This reverses the direction of charging current. It means capacitor will also have to reversed, if it is electrolytic one. The emitter of the transistor must be connected to virtual ground (the inverting input terminal of op-amp). To allow the capacitor to discharge from left to right, NPN transistor would have to be replaced by PNP transistor. In this case, a zero or positive control input would keep the PNP transistor off, while a negative control input would be required to turn the transistor on.

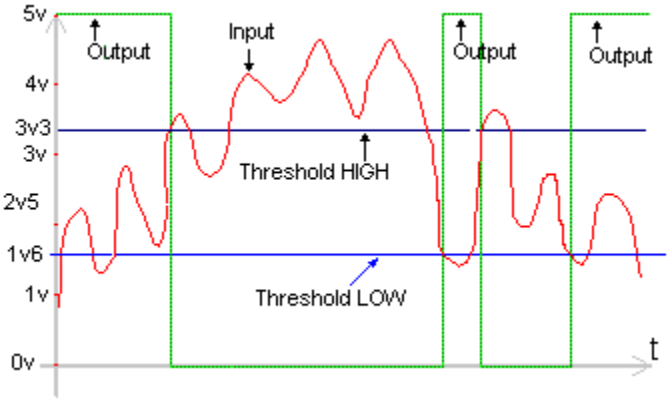
4.CIRCUIT DIAGRAM :

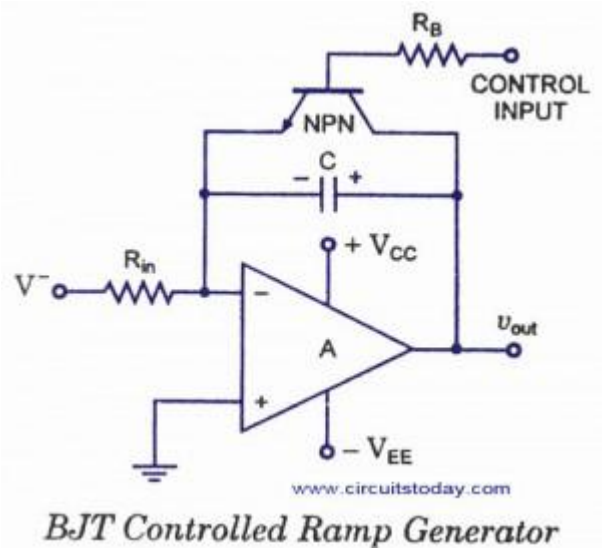


Control Input Signals Effect on The Ramp Generator's Output



THE OP-AMP AS A SCHMITT TRIGGER





BJT Controlled Ramp Generator

5. RESULT : The characteristics of sawtooth and ramp wave generator is studied.

6. PRECAUTIONS : 1.The connections should be tight.

2. Switch on power supply after checking the circui

EXPERIMENT NO 13

1.OBJECTIVE : Preparation of adjustable timer using op amp.

2.MATERIAL REQUIRED : adjustable timer using op amp.

3.THEORY : The 555 timer is an extremely versatile integrated circuit which can be used to build lots of different circuits. You can use the 555 effectively without understanding the function of each pin in detail.

Frequently, the 555 is used in astable mode to generate a continuous series of pulses, but you can also use the 555 to make a one-shot or monostable circuit. The 555 can source or sink 200 mA of output current, and is capable of driving wide range of output devices.

The design formula for the frequency of the pulses is:

$$f = \frac{1.44}{(R1 + 2R2) \times C}$$

The period, *t*, of the pulses is given by:

$$t = \frac{1}{f} = 0.69(R1 + 2R2) \times C$$

The HIGH and LOW times of each pulse can be calculated from:

$$\text{HIGH time} = 0.69(R1 + R2) \times C$$

$$\text{LOW time} = 0.69(R2 \times C)$$

The duty cycle of the waveform, usually expressed as a percentage, is given by:

$$\text{duty cycle} = \frac{\text{HIGH time}}{\text{pulse period time}}$$

An alternative measurement of HIGH and LOW times is the mark space ratio:

$$\text{mark space ratio} = \frac{\text{HIGH time}}{\text{LOW time}}$$

Before calculating a frequency, you should know that it is usual to make *R*1=1 kΩ because this helps to give the output pulses a duty cycle close to 50%, that is, the HIGH and LOW times of the pulses are approximately equal.

Remember that design formulae work in fundamental units. However, it is often more convenient to work with other combinations of units:

With *R* values in MΩ and *C* values in μF, the frequency will be in Hz.
Alternatively, with *R* values in kΩ and *C* values in μF, frequencies will be in kHz.

Suppose you want to design a circuit to produce a frequency of approximately 1 kHz for an alarm application. What values of *R*1, *R*2 and *C* should you use?

*R*1 should be 1kΩ, as already explained. This leaves you with the task of selecting values for *R*2 and *C*. The best thing to do is to rearrange the design formula so that the *R* values are on the right hand side:

$$R1 + 2R2 = \frac{1.44}{f \times C}$$

Now substitute for *R*1 and *f* :

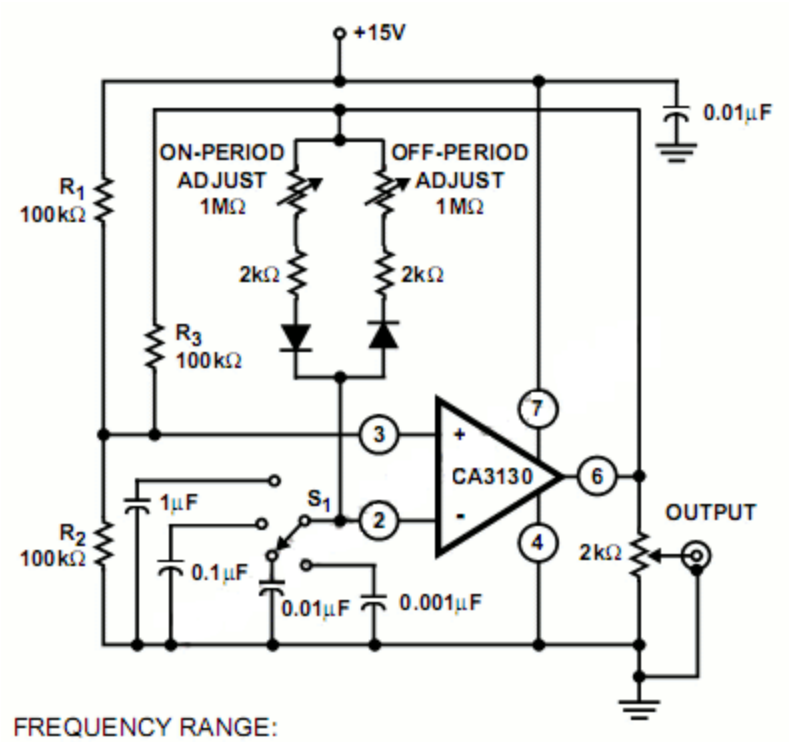
$$1 + 2R2 = \frac{1.44}{1 \times C}$$

You are using *R* values in kΩ and *f* values in kHz, so *C* values will be in μF.To make further progress, you must choose a value for *C*. At the same time, it is important to remember that practical values for *R*2 are between 1 kΩ and 1MΩ.

Suppose you choose *C* = 10 nF = 0.01 μF:

$$1 + 2R2 = \frac{1.44}{0.01} = 144$$

4.CIRCUIT DIAGRAM :



FREQUENCY RANGE:

POSITION OF S_1	PULSE PERIOD
0.001μF	4μs to 1ms
0.01μF	40μs to 10ms
0.1μF	0.4ms to 100ms
1μF	4ms to 1s

5. RESULT : The operation of adjustable timer is studied.

6. PRECAUTIONS

1. The Kit Should be handle with care fully.
2. The wire should not be touch .
3. .Take the carefully reading.

EXPERIMENT NO 14

1. OBJECTIVE : Oscillator using op amp (a) Weins Bridge oscillator (b) R C Phase shift oscillator.

2.MATERIAL REQUIRED : 1. Transistor 1
2. Resistor 8
3. Capacitor 4
4. Dc voltage source 1

3. THEORY : (a) Weins bridge Oscillator : A Wien bridge oscillator is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The circuit is based on an electrical network originally developed by Max Wien in 1891. The bridge comprises four resistors and two capacitors. It can also be viewed as a positive feedback system combined with a bandpass filter. Wien did not have a means of developing electronic gain so a workable oscillator could not be realized.

If a voltage source is applied directly to the input of an ideal amplifier with feedback, the input current will be:

$$i_{in} = \frac{v_{in} - v_{out}}{Z_f}$$

Where v_{in} is the input voltage, v_{out} is the output voltage, and Z_f is the feedback impedance. If the voltage gain of the amplifier is defined as:

$$A_v = \frac{v_{out}}{v_{in}}$$

And the input admittance is defined as:

$$Y_i = \frac{i_{in}}{v_{in}}$$

Input admittance can be rewritten as:

$$Y_i = \frac{1 - A_v}{Z_f}$$

For the Wien bridge, Z_f is given by:

$$Z_f = R + \frac{1}{j\omega C}$$

$$Y_i = \frac{(1 - A_v)\left(\omega^2 C^2 R + j\omega C\right)}{1 + (\omega C R)^2}$$

If A_v is greater than 1, the input admittance is a negative resistance in parallel with an inductance. The inductance is:

$$L_{in} = \frac{\omega^2 C^2 R^2 + 1}{\omega^2 C\left(A_v - 1\right)}$$

If a capacitor with the same value of C is placed in parallel with the input, the circuit has a natural resonance at:

$$\omega = \frac{1}{\sqrt{L_{in} C}}$$

Substituting and solving for inductance yields:

$$L_{in} = \frac{R^2 C}{A_v - 2}$$

If A_v is chosen to be 3:

$L_{in} = R^2 C$

Substituting this value yields:

$$\omega = \frac{1}{RC}$$

Or:

$$f = \frac{1}{2\pi RC}$$

Similarly, the input resistance at the frequency above is:

$$R_{in} = \frac{-2R}{A_v - 1}$$

For $A_v = 3$:

$R_{in} = -R$

If a resistor is placed in parallel with the amplifier input, it will cancel some of the negative resistance. If the net resistance is negative, amplitude will grow until

clipping occurs. Similarly, if the net resistance is positive, oscillation amplitude will decay. If a resistance is added in parallel with exactly the value of *R*, the net resistance will be infinite and the circuit can sustain stable oscillation at any amplitude allowed by the amplifier.

Notice that increasing the gain makes the net resistance more negative, which increases amplitude. If gain is reduced to exactly 3 when a suitable amplitude is reached, stable, low distortion oscillations will result. Amplitude stabilization circuits typically increase gain until a suitable output amplitude is reached. As long as *R*, *C*, and the amplifier are linear, distortion will be minimal.

(b) RC Phase shift Oscillator : An oscillator is a circuit, which generates ac output signal without giving any input ac signal. This circuit is usually applied for audio frequencies only. The basic requirement for an oscillator is positive feedback. The operation of the RC Phase Shift Oscillator can be explained as follows. The starting voltage is provided by noise, which is produced due to random motion of electrons in resistors used in the circuit. The noise voltage contains almost all the sinusoidal frequencies. This low amplitude noise voltage gets amplified and appears at the output terminals. The amplified noise drives the feedback network which is the phase shift network. Because of this the feedback voltage is maximum at a particular frequency, which in turn represents the frequency of oscillation. Furthermore, the phase shift required for positive feedback is correct at this frequency only. The voltage gain of the amplifier with positive feedback . The gain becomes infinity means that there is output without any input. i.e. the amplifier becomes an oscillator. This condition is known as the Barkhausen criterion of oscillation. Thus the output contains only a single sinusoidal frequency. In the beginning, as the oscillator is switched on, the loop gain A is greater than unity. The oscillations build up. Once a suitable level is reached the gain of the amplifier decreases, and the value of the loop gain decreases to unity. So the constant level oscillations are maintained. Satisfying the above conditions of oscillation the value of *R* and *C* for the phase shift network is selected such that each *RC* combination produces a phase shift of 60°. Thus the total phase shift produced by the three *RC* networks is 180°. Therefore at the specific frequency f_o the total phase shift from the base of the transistor around the circuit and back to the base is 360° thereby satisfying *Barkhausen criterion*. We select $R_1=R_2=R_3=R$ and $C_1=C_2=C_3=C$

The mathematics for calculating the oscillation frequency and oscillation criterion for this circuit are surprisingly complex, due to each R-C stage loading the previous ones. The calculations are greatly simplified by setting all the resistors (except the negative feedback resistor) and all the capacitors to the same values. In the diagram, if R1 = R2 = R3 = *R*, and C1 = C2 = C3 = *C*, then:

$$f_{\text{oscillation}} = \frac{1}{2\pi RC\sqrt{6}}$$

and the oscillation criterion is: $R_{\text{feedback}} = 29(R)$

Without the simplification of all the resistors and capacitors having the same values, the calculations become more complex:

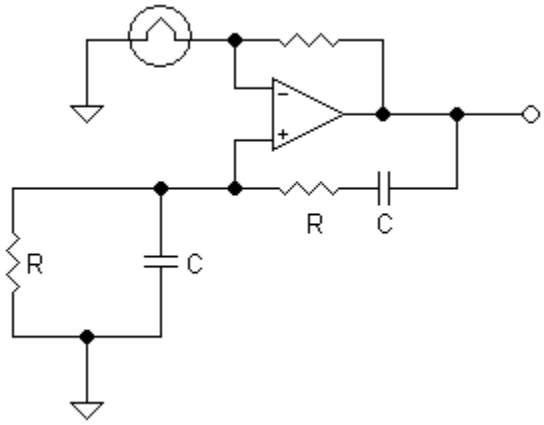
$$f_{\text{oscillation}} = \frac{1}{2\pi\sqrt{R_2R_3(C_1C_2 + C_1C_3 + C_2C_3) + R_1R_3(C_1C_2 + C_1C_3) + R_1R_2C_1C_2}}$$

Oscillation criterion:

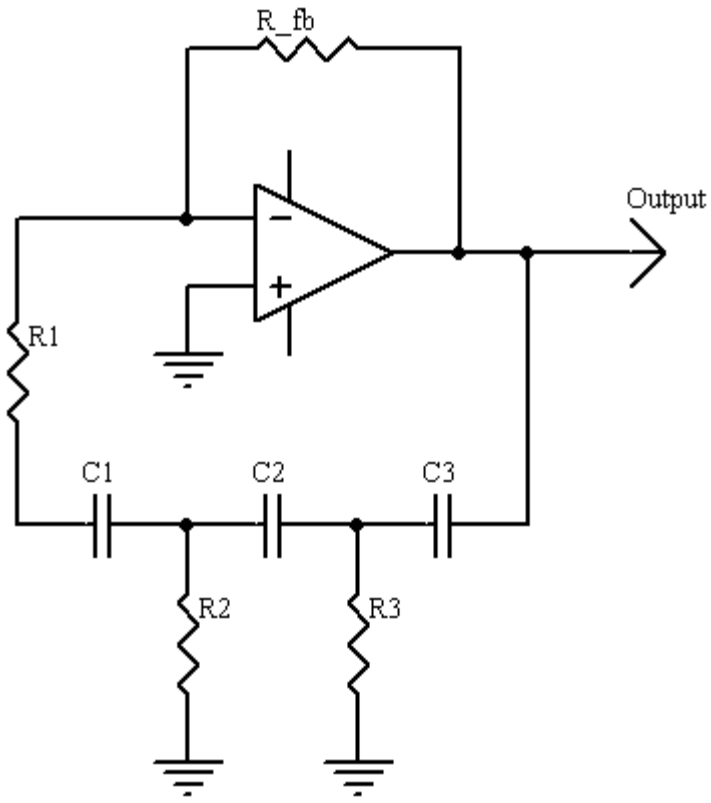
$$R_{\text{feedback}} = 2(R_1 + R_2 + R_3) + \frac{2R_1R_3}{R_2} + \frac{C_2R_2 + C_2R_3 + C_3R_3}{C_1}$$
$$+\frac{2C_1R_1 + C_1R_2 + C_3R_3}{C_2} + \frac{2C_1R_1 + 2C_2R_1 + C_1R_2 + C_2R_2 + C_2R_3}{C_3}$$
$$+\frac{C_1R_1^2 + C_3R_1R_3}{C_2R_2} + \frac{C_2R_1R_3 + C_1R_1^2}{C_3R_2} + \frac{C_1R_1^2 + C_1R_1R_2 + C_2R_1R_2}{C_3R_3}$$

A version of this circuit can be made by putting an op-amp buffer between each R-C stage which simplifies the calculations. The voltage gain of the inverting channel is always unity.When the oscillation frequency is high enough to be near the amplifier's cutoff frequency, the amplifier will contribute significant phase shift itself, which will add to the phase shift of the feedback network. Therefore the circuit will oscillate at a frequency at which the phase shift of the feedback filter is less than 180 degrees.

4.CIRCUIT DIAGRAM :



Classic Wien bridge oscillator



RC Phase shift oscillator

5.RESULT : The operation of phase shift and weins bridge oscillator is studied.

6.PRECAUTIONS :

1.Connections of circuit should be tight.

2. power supply should be switched on after checking circuit.

EXPERIMENT NO 15

1.OBJECTIVE : Clamper and chopper operation (a) positive and negative clamper (b) positive and negative clipper.

2. MATERIAL REQUIRED : Clipper and clamper circuit.

3. THEORY : In a positive clipper, the positive half cycles of the input voltage will be removed. The circuit arrangements for a positive clipper are illustrated in the figure given below.

As shown in the figure, the diode is kept in series with the load. During the positive half cycle of the input waveform, the diode 'D' is reverse biased, which maintains the output voltage at 0 Volts. Thus causes the positive half cycle to be clipped off. During the negative half cycle of the input, the diode is forward biased and so the negative half cycle appears across the output.

In Figure (b), the diode is kept in parallel with the load. This is the diagram of a positive shunt clipper circuit. During the positive half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the positive half cycles is zero, as shown in the output waveform. During the negative half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance R_L if R is much smaller than R_L

Actually the circuit behaves as a voltage divider with an output voltage of $[R_L / R+ R_L] V_{max} = -V_{max}$ when $R_L >> R$

The negative clipping circuit is almost same as the positive clipping circuit, with only one difference. If the diode in figures (a) and (b) is reconnected with reversed polarity, the circuits will become for a negative series clipper and negative shunt clipper respectively. The negative series and negative shunt clippers are shown in figures (a) and (b) as given below.

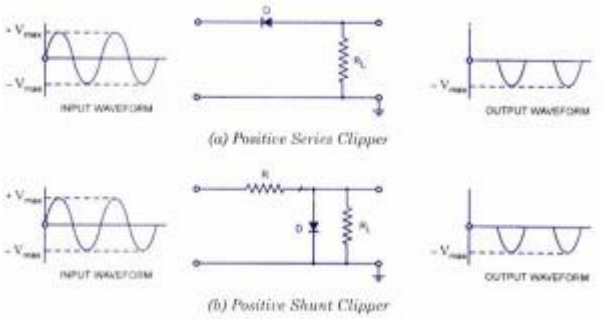
A clamper is an electronic circuit that prevents a signal from exceeding a certain defined magnitude by shifting its DC value. The clamper does not restrict the peak-to-peak excursion of the signal, but moves it up or down by a fixed value. A diode clamp (a simple, common type) relies on a diode, which conducts electric current in only one direction; resistors and capacitors in the circuit are used to maintain an altered dc level at the clamper output.
Positive unbiased

Capacitor to the peak value of V_{IN}. During the negative cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the In the negative cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak positive value of V_{IN}. During the positive cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the

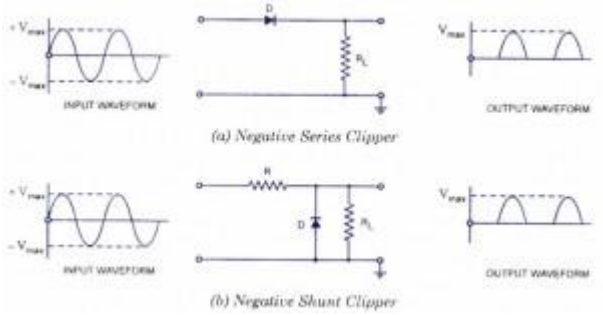
voltage stored in the capacitor plus the input voltage again, so $V_{OUT} = 2V_{IN.}$ A positive biased voltage clamp is identical to an equivalent unbiased clamp but with the output voltage offset by the bias amount V_{BIAS}. Thus, $V_{OUT} = 2V_{IN} + V_{BIAS}$

Negative biased : A negative unbiased clamp is the opposite of the equivalent positive clamp. In the positive cycle of the input AC signal, the diode is forward biased and conducts, charging the input voltage again, so $V_{OUT} = -2V_{IN.}$ A negative biased voltage clamp is likewise identical to an equivalent unbiased clamp but with the output voltage offset in the negative direction by the bias amount V_{BIAS}. Thus, $V_{OUT} = -2V_{IN} - V_{BIAS}$

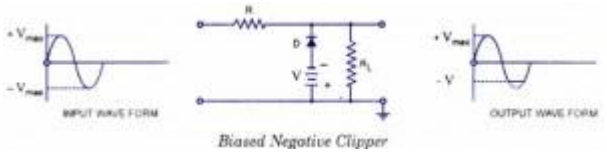
4.CIRCUIT DIAGRAM :



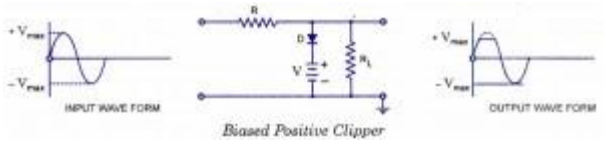
Positive Series Clipper and Positive Shunt clipper



Negative Series Clipper and Negative Shunt clipper



Biased Negative Clipper



Biased Positive Clipper

5.RESULT : The operation of clipper and clamper is studied.

6.PRECAUTIONS :

1.Connections of circuit should be tight.

2. power supply should be switched on after checking circuit.

EXPERIMENT NO 16

1.OBJECTIVE : Sample and hold circuit operation .

2.MATERIAL REQUIRED : Sample and hold circuit , connecting wire.

3.THEORY : In electronics, a **sample and hold** (**S/H**, also "follow-and-hold") circuit is an analog devicethat samples (captures, grabs) the voltage of a continuously varying analog signal and holds (locks, freezes) its value at a constant level for a specified minimal period of time. Sample and hold circuits and related peak detectors are the elementary analog memory devices. They are typically used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process.[

A typical sample and hold circuit stores electric charge in a capacitor and contains at least one fast FET switch and at least one operational amplifier. To sample the input signal the switch connects the capacitor to the output of a buffer amplifier. The buffer amplifier charges or discharges the capacitor so that the voltage across the capacitor is practically equal, or proportional to, input voltage. In hold mode the switch disconnects the capacitor from the buffer. The capacitor is invariably discharged by its own leakage currents and useful load currents, which makes the circuit inherently volatile, but the loss of voltage (*voltage drop*) within a specified hold time remains within an acceptable error margin.

The reasons for using such a circuit are varied. In some kinds of analog-to-digital converters, the input is often compared to a voltage generated internally from a digital-to-analog converter. The circuit tries a series of values and stops converting once the voltages are "the same" within some defined error margin. If the input value was permitted to change during this comparison process, the resulting conversion would be inaccurate and possibly completely unrelated to the true input value. Such successive approximation converters will often incorporate internal sample and hold circuitry. In addition, sample and hold circuits are often used when multiple samples need to be measured at the same time. Each value is sampled and held, using a common sample clock.

In order that the input voltage is held constant for all practical purposes, it is essential that the capacitor have very low leakage, and that it not be loaded to any significant degree which calls for a very high input impedance.

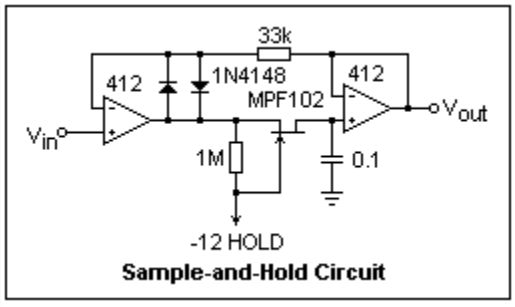
A true sample and hold circuit is connected to the buffer for a short period of time; a *track and hold* circuit is designed to track input continuously.

An illustrative sample-and-hold circuit is shown at the left, made from discrete components. The dual op-amps in an LM412 are ideal for the purpose, because their input bias currents are practically zero. An MPF102 is used to isolate the capacitor from the source used to charge it. For our purposes, we can command sample and hold by connecting a wire manually to -12 for HOLD, and leaving it disconnected for SAMPLE. For a practical circuit, we would make better arrangements for the control. Note the back-to-back signal diodes at the output of the left-hand op-amp (any diodes can be used). The purpose of these diodes is to "catch" the output when the feedback loop is broken when the JFET turns OFF. The 33k resistor isolates this action from the output feedback loop. If these diodes are not present, the op-amp saturates at the supply rail and the JFET will not turn off. Test the circuit, make sure it HOLDs properly, and observed the droop of the output. I found a droop of 0.23V in 5 minutes, or a rate of just 0.77 mV/s, corresponding to a leakage of 77 pA! This is really pretty good.

The choice of hold capacitor is important. The leakage of electrolytics and the transient behavior of ceramics rule them out completely in this application. The best choice is probably polypropylene, which I used, and after that polystyrene or Mylar. Polycarbonate is much inferior to all of these. The greatest problem (after leakage, which should be practically zero) is *dielectric hysteresis* in which the voltage changes on charge and discharge are not the same. There is also *dielectric absorption*, where there is a "memory" of past states. A capacitor freshly discharged may acquire a small voltage as time goes by. All of these phenomena are the result of the complexity of dielectric structure and behavior.

Some properties of sample-and-hold circuits are important in critical, dynamic applications. The *hold step* is the change in output voltage when the circut is switched OFF, the result of various capacitive effects. The settling time is the time required after the HOLD command for the output to stabilize. The aperture time is the time after the HOLD command at which changes in the input have no effect. The aquisition time is the time at which the ouput settles after a change at the input. Finally, the *dynamic sampling error* is the difference between the voltage held and the instantaneous input voltage at the instant of the HOLD command. Our experiment is not set up to measure any of these accurately. Hold steps are on the order of mV, aquisition times of µs.

4.CIRCUIT DIAGRAM :



Sample-and-Hold Circuit

A simplified sample and hold circuit diagram. AI is an analog input, AO — an analog output, C — a control signal.

5.RESULT :The operation of sample and hold circuit is studied.

6.PRECAUTIONS :

1.Connections of circuit should be tight.

2. power supply should be switched on after checking circuit.

EXPERIMENT NO17

1.OBJECTIVE : Precision rectifier using an op amp and voltage regulations.

2.MATERIAL REQUIRED : Precision rectifier, connecting wires.

3.THEORY :Half Wave Precision Rectifiers

There are many applications for precision rectifiers, and while most are suitable for use in audio circuits, I thought it best to make this the first ESP Application Note. While some of the existing projects in the audio section have a rather tenuous link to audio, this information is more likely to be used for instrumentation purposes than pure audio applications.

Typically, the precision rectifier is not commonly used to drive analogue meter movements, as there are usually much simpler methods to drive floating loads such as meters. Precision rectifiers are more common where there is some degree of post processing needed, feeding the side chain of compressors and limiters, or to drive digital meters.

There are several different types of precision rectifier, but before we look any further, it is necessary to explain what a precision rectifier actually is. In its simplest form, a half wave precision rectifier is implemented using an opamp, and includes the diode in the feedback loop. This effectively cancels the forward voltage drop of the diode, so very low level signals (well below the diode's forward voltage) can still be rectified with minimal error.

The most basic form is shown in Figure 1, and while it does work, it has some serious limitations. The main one is speed - it will not work well with high frequency signals. To understand the reason, we need to examine the circuit closely. This knowledge applies to all subsequent circuits, and explains the reason for the apparent complexity. For a low frequency positive input signal, 100% negative feedback is applied when the diode conducts. The forward voltage is effectively removed by the feedback, and the inverting input follows the positive half of the input signal almost perfectly. When the input signal becomes negative, the op amp has no feedback at all, so the output pin of the opamp swings negative as far as it can. Assuming 15V supplies, that means perhaps -14V on the opamp output.

When the input signal becomes positive again, the opamp's output voltage will take a finite time to swing back to zero, then to forward bias the diode and produce an output. This time is determined by the opamp's slew rate, and even a very fast opamp will be limited to low frequencies - especially for low input levels. The test voltage for the waveforms shown was 20mV at 1kHz. Although the circuit does work very well, it is limited to relatively low frequencies (less than 10kHz) and only becomes acceptably linear above 10mV or so (opamp dependent).Note the oscillation at the rectified output. This is (more or less) real, and was confirmed with an actual (as opposed to simulated) circuit. This is the result of the opamp becoming open-loop with negative inputs. In most cases it is not actually a problem.

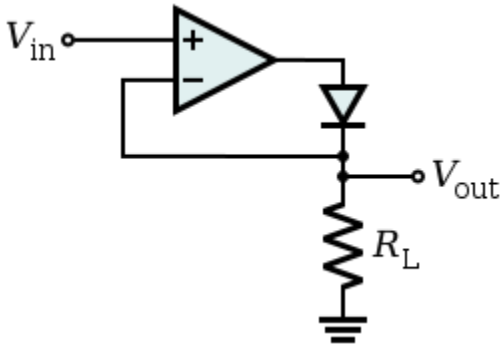
Full Wave Precision Rectifiers

Figure 4 shows the standard full wave version of the precision rectifier. This circuit is very common, and is pretty much the textbook version. It has been around for a very long time now, and I would include a reference to it if I knew where it originated. The tolerance of R2, 3, 4 and 5 is critical for good

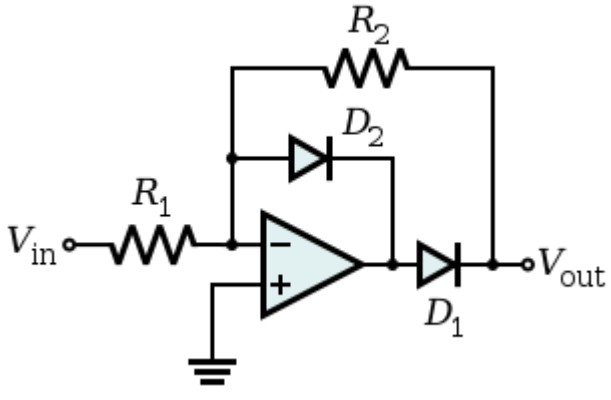
performance, and all four resistors should be 1% or better. Note that the diodes have been reversed to obtain a positive rectified signal. The second stage inverts the signal polarity. To obtain improved high frequency response, the resistor values should be reduced.

A simple precision rectifier circuit was published by Intersil [2]. This is an interesting variation, because it uses a single supply opamp but still gives full-wave rectification, with both input and output earth (ground) referenced. Unfortunately, the specified opamp is not especially common, although other devices could be used. The CA3140 is a reasonably fast opamp, having a slew rate of 7V/us. I will leave it to the reader to determine suitable types (other than that suggested below). The essential features are that the two inputs must be able to operate at below zero volts (typically -0.5V), and the output must also include close to zero volts.

4.CIRCUIT DIAGRAM :



A simple precision rectifier circuit.



An improved precision rectifier circuit

5.RESULT : The operation of precision rectifier is studied.

6.PRECAUTIONS : 1.Connections should be tight.

2.power supply should be switched on after checking the circuit.

EXPERIMENT NO 18

1.OBJECTIVE : Measurement VCO sensitivity ,linearity and free running frequency

2.MATERIAL REQUIRED : VCO Circuit, CRO.

3.THEORY : A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The frequency of oscillation is varied by the applied DC voltage, while modulating signals may also be fed into the VCO to cause frequency modulation (FM) or phase modulation (PM); a VCO with digital pulse output may similarly have its repetition rate (FSK, PSK) or pulse width modulated (PWM).

This voltage-controlled oscillator circuit is very compact and has a good linearity. The author said that the precision could be better than 0.01% If this circuit is properly constructed. Moreover, this circuit gives three different output waveforms: square, triangle, and sawtooth. This three waveform is important for music synthesizer and measurement devices. Here is the circuit's schematic diagram:

The oscillator consist of a mixer (U1) and a comparator with hysteresis U2. if U2 has positive output (+15V) then FET Q1 will be conducting, and if the output is negative then the FET will be open, in other words, the FET will function as an electronic switch. The voltage at pin 2 U1 will be kept constant at 1/3 Vin (set by R3 R4) by op-amp feedback mechanism. If Q1 is switched off then the capacitor C1 will be charged from Vin to U1 out through R1 and R2. The effect of this charging is that the voltage seen at U1 (pin 6) output will increase. After this pin 6 U1 voltage reach the upper threshold of U2 Schmidt trigger (the hysteresis is set by R6 R7), the U2 output will swing to V+ and switch on the Q1 switch. After Q1 switched on, the capacitor C1 current now reverse it's direction, discharging, and the U1 output will be decreasing. After reaching the lower threshold level of U2 Schmidt trigger then U2 output will swing to V-, switch the Q1 off and the restart the cycle.

The sawtooth output will be a triangle wave with same frequency as the square wave output when SW1 is open. If SW1 is closed then the C1 capacitor discharging will be very fast and the triangle output will change into sawtooth waveform with two times higher frequency. The amplitude of sawtooth or triangle output will be about (+ -) 8.3V, and the square output will be (+ -) 15 V. Except for R5, R9, and R10 those require no high precision, all resistors should be 1% tolerance or better.

The output frequency will follow the equation:

$f = (Vin \cdot R6)/(180.R7.R2.C1)$,

where the frequency is in Hz, capacitance in Farad, and resistance in Ohm. Vin is the control voltage in Volt. With the values shown in the schematic diagram, the voltage-frequency conversion rate will be 357Hz/Volt. Setting the R11

potentiometer is done by shorting the negative and positive inputs of U1 to ground and adjust R11 to give zero volt reading at U1 output (pin 6). [circuit 's schematic diagram source: elector]

A voltage-controlled crystal oscillator (VCXO) is used when the frequency of operation needs to be adjusted only finely. The frequency of a voltage-controlled crystal oscillator can be varied only by typically a few tens of parts per million (ppm), because the high Q factor of the crystals allows "pulling" over only a small range of frequencies.

There are two reasons for using a VCXO:

- To adjust the output frequency to match (or perhaps be some exact multiple of) an accurate external reference.
- Where the oscillator drives equipment that may generate radio-frequency interference, adding a varying voltage to its control input can disperse the interference spectrum to make it less objectionable. See spread-spectrum clock generation.

A temperature-compensated VCXO (TCVCXO) incorporates components that partially correct the dependence on temperature of the resonant frequency of the crystal. A smaller range of voltage control then suffices to stabilize the oscillator frequency in applications where temperature varies, such as heat buildup inside a transmitter.

VCO time-domain equations

Tuning range, tuning gain and phase noise are the most important factors of the basic design of a VCO. Generally low phase noise is preferred in the VCO. The important elements that determine the phase noise of an oscillator are the material[1], transistor's flicker noise corner frequency, the loaded Q of the resonator and the final signal to noise ratio.

Most commonly used VCO circuits are the Clapp and Colpitts oscillators. The more widely used oscillator of the two is Colpitts and these oscillators are very similar in configuration.

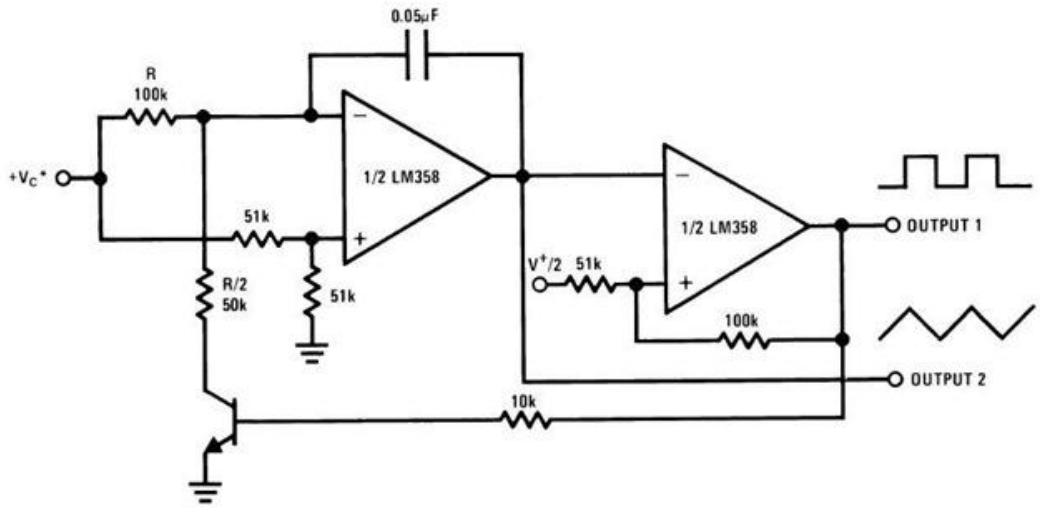
VCOs generally have the lowest Q-factor of the used oscillators, and so suffer more jitter than the other types. The jitter can be made low enough for many applications (such as driving an ASIC), in which case VCOs enjoy the advantages of having no off-chip components (expensive) or on-chip inductors (low yields on generic CMOS processes). These oscillators also have larger tuning ranges than the other kinds, which improves yield and is sometimes a feature of the end product (for instance, the dot clock on a graphics card which drives a wide range of monitors).

Applications

VCOs are used in:

- Electronic jamming equipment
- Function generators,
- The production of electronic music, to generate variable tones,
- Phase-locked loops,
- Frequency synthesizers used in communication equipment.

4.CIRCUIT DIAGRAM :



Voltage-controlled oscillator schematic - audio

5.RESULT : The operation of VCO is studied.

6.PRECAUTIONS :1.Connections should be tight.

2. switch on power supply after checking the circuit .

EXPERIMENT NO 19

1.OBJECTIVE : Phase lock loop as frequency multiplier .

2.MATERIAL REQUIRED : PLL , CRO

3.THEORY : A phase-locked loop or phase lock loop (PLL) is a control system that tries to generate an output signal whose phase is related to the phase of the input "reference" signal. It is an electronic circuit consisting of a variable frequency oscillator and a phase detector. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. The signal from the phase detector is used to control the oscillator in a feedback loop.

Frequency is the derivative of phase. Keeping the input and output phase in lock step implies keeping the input and output frequencies in lock step. Consequently, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. The former property is used for demodulation, and the latter property is used for indirect frequency synthesis.

Phase-locked loops are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

Performance parameters

- Type and order
- Lock range: The frequency range the PLL is able to stay locked. Mainly defined by the VCO range.
- Capture range: The frequency range the PLL is able to lock-in, starting from unlocked condition. This range is usually smaller than the lock range and will depend e.g. on phase detector.
- Loop bandwidth: Defining the speed of the control loop.
- Transient response: Like overshoot and settling time to a certain accuracy (like 50ppm).
- Steady-state errors: Like remaining phase or timing error
- Output spectrum purity: Like sidebands generated from a certain VCO tuning voltage ripple.
- Phase-noise: Defined by noise energy in a certain frequency band (like 10kHz offset from carrier). Highly dependent on VCO phase-noise, PLL bandwidth, etc.
- General parameters: Such as power consumption, supply voltage range, output amplitude, etc.

A phase detector compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a VCO which creates an output phase. The output is fed through an optional divider back to the input of the system, producing a negative

feedback loop. If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase at the other input. This input is called the reference.

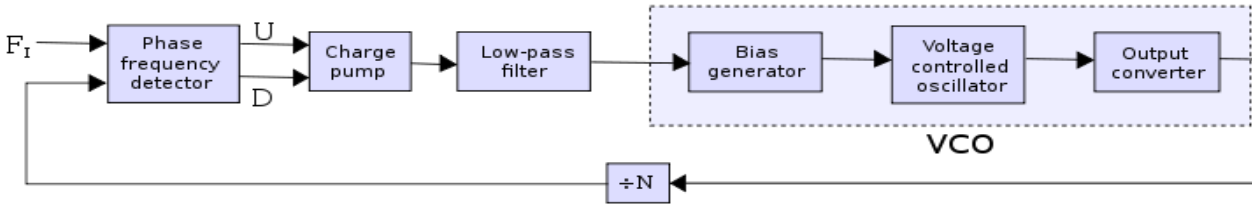
Analog phase locked loops are generally built with an analog phase detector, low pass filter and VCO placed in a negative feedback configuration. A digital phase locked loop uses a digital phase detector; it may also have a divider in the feedback path or in the reference path, or both, in order to make the PLL's output signal frequency a rational multiple of the reference frequency. A non-integer multiple of the reference frequency can also be created by replacing the simple divide-by-N counter in the feedback path with a programmable pulse swallowing counter. This technique is usually referred to as a fractional-N synthesizer or fractional-N PLL.[The oscillator generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. If the phase from the oscillator falls behind that of the reference, the phase detector changes the control voltage of the oscillator so that it speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs.

Depending on the application, either the output of the controlled oscillator, or the control signal to the oscillator, provides the useful output of the PLL system.

The block diagram of a frequency muliplier (or synthesizer) is shown in figure. In this circuit, a frequency divider is inserted between the output of the VCO and the phase comparator (PC) so that the loop signal to the PC is at frequency f_{OUT} while the output of VCO is N f_{OUT}. This output is a multiple of the input frequency as long as the loop is in lock. The desired amount of multiplication can be obtained by selecting a proper divide- by N network where N is an integer. Figure shows this function performed by a 7490 configured as a divide-by-4 circuit.

In this case the input V_{in} at frequency $/_{in}$ is compared with the output frequency f_{OUT} at pin 5. An output at N f_{OUT} (4 f_{OUT} in this case) is connected through an inverter circuit to give an input at pin 14 of the 7490, which varies between 0 and + 5 V. Using the output at pin 9, which is one-fourth of that at the input to the 7490, the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock.Since the VCO can be adjusted over a limited range from its centre frequency, it may become necessary to change the VCO frequency whenever the divider value is changed.For verification of the circuit operation, one must determine the input frequency range and then adjust the free running f_{OUT} of the VCO by means of R_1 and C_1 so that the output frequency of the 7490 divider is midway within the predetermined input frequency range. The output of VCO should now be equal to 4 f_{in}.

4..CIRCUIT DIAGRAM :



Digital phase-locked loop block diagram

5.RESULT : The operation of PLL is studied.

6.PRECAUTIONS : 1. Connections should be tight.

2. power supply should be on after checking circuit

EXPERIMENT NO 20

1.OBJECTIVE : Calculate the duty cycle of PWM.

2.MATERIAL REQUIRED : PWM, CRO

3.THEORY : Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is.

The PWM switching frequency has to be much faster than what would affect the load, which is to say the device that uses the power. Typically switchings have to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

The term *duty cycle* describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

PWM has also been used in certain communication systems where its duty cycle has been used to convey information over a communications channel.

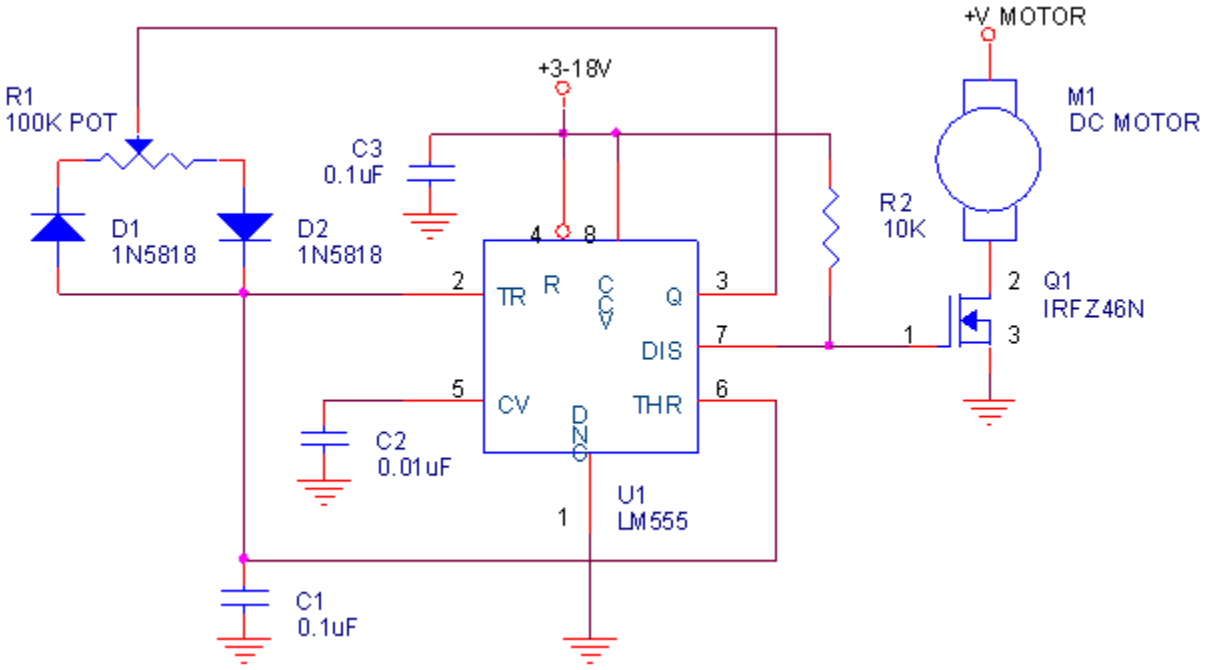
lse-width modulation uses a rectangular pulse wave whose pulse width is modulated resulting in the variation of the average value of the waveform. If we consider a pulse waveform $f(t)$ with a low value y_{min}, a high value y_{max} and a duty cycle D (see figure 1), the average value of the waveform is given by:

A simple method to generate the PWM pulse train corresponding to a given signal is the intersective PWM: the signal (here the green sinewave) is compared

with a sawtooth waveform (blue). When the latter is less than the former, the PWM signal (magenta) is in high state (1). Otherwise it is in the low state (0).

The simplest way to generate a PWM signal is the intersective method, which requires only a sawtooth or a triangle waveform (easily generated using a simple oscillator) and a comparator. When the value of the reference signal (the green sine wave in figure 2) is more than the modulation waveform (blue), the PWM signal (magenta) is in the high state, otherwise it is in the low state.

4.CIRCUIT DIAGRAM :



PWM CIRCUIT

5.RESULT :The operation of PWM is studied.

6.PRECAUTIONS : 1. Connections should be tight.

2. power supply should be on after checking circuit.

EXPERIMENT NO 21

1.OBJECTIVE : A/D conveter.

2.MATERIAL REQUIRED : A/D Converter.

3.THEORY : Analog-to-Digital converters - a.k.a. A/D converters - are widely used by many engineers and scientists of all types, often without their realizing it. Whenever they make a measurement of a voltage, and that measurement is taken into a computer, an A/D is used.

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device which converts a continuous quantity to a discrete time digital representation. An ADC may also provide an isolated measurement. The reverse operation is performed by a digital-to-analog converter (DAC).

Typically, an ADC is an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. However, some non-electronic or only partially electronic devices, such as rotary encoders, can also be considered ADCs.

Flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, $2^N - 1$, doubles with each additional bit, requiring a large expensive circuit. ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches on the output (by outputting an out-of-sequence code). Scaling to newer sub micrometre technologies does not help as the device mismatch is the dominant design limitation. They are often used for video, wideband communications or other fast signals in optical storage.

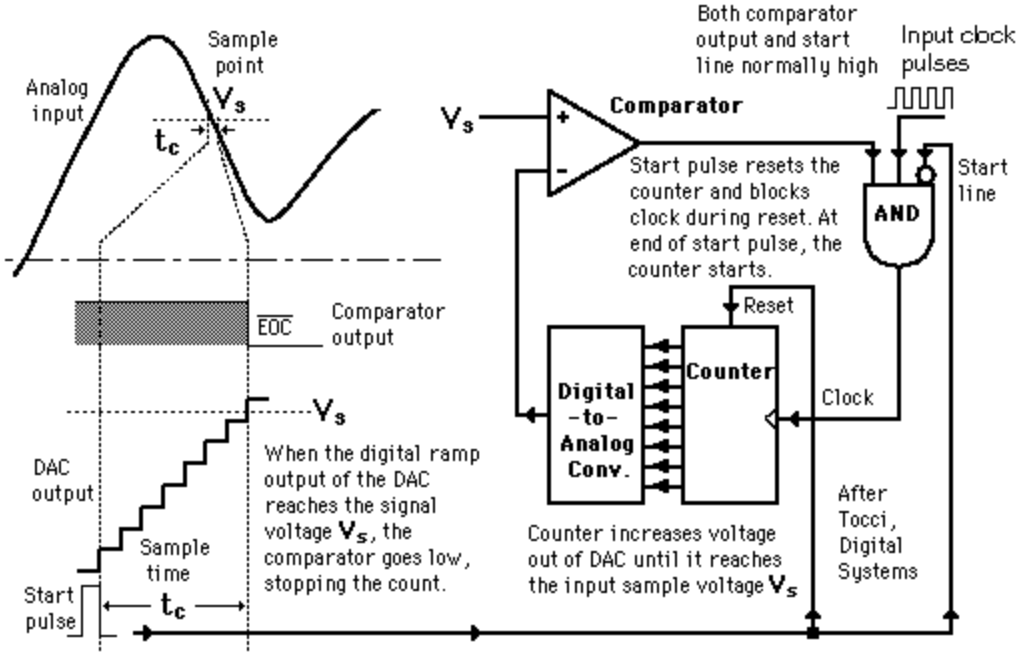
A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons. For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V

(halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called bit-weighting conversion, and is similar to a binary search. The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.

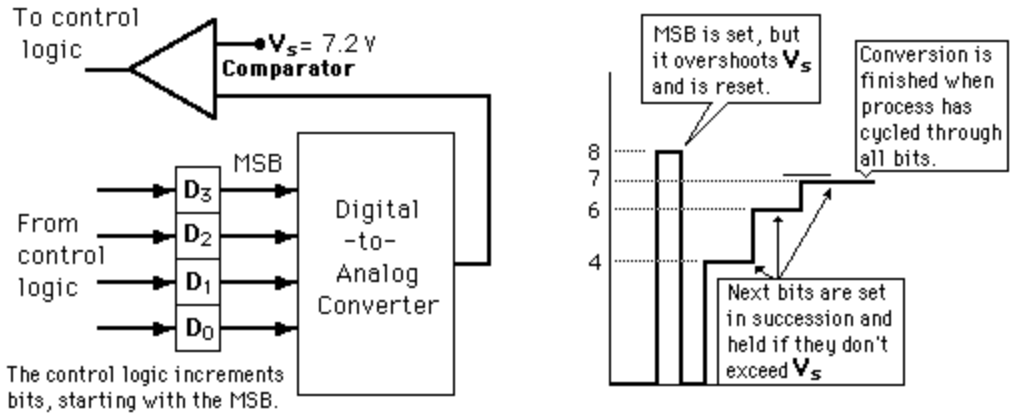
A ramp-compare ADC produces a saw-tooth signal that ramps up or down then quickly returns to zero. When the ramp starts, a timer starts counting. When the ramp voltage matches the input, a comparator fires, and the timer's value is recorded. Timed ramp converters require the least number of transistors. The ramp time is sensitive to temperature because the circuit generating the ramp is often just some simple oscillator. There are two solutions: use a clocked counter driving a DAC and then use the comparator to preserve the counter's value, or calibrate the timed ramp. A special advantage of the ramp-compare system is that comparing a second signal just requires another comparator, and another register to store the voltage value. A very simple (non-linear) ramp-converter can be implemented with a microcontroller and one resistor and capacitor.[10] Vice versa, a filled capacitor can be taken from an integrator, time-to-amplitude converter, phase detector, sample and hold circuit, or peak and hold circuit and discharged. This has the advantage that a slow comparator cannot be disturbed by fast input changes.

An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.

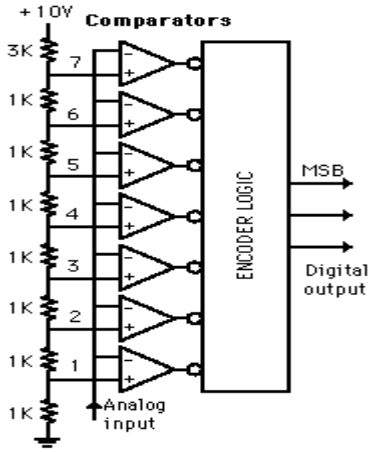
4.CIRCUIT DIAGRAM :



Digital Ramp ADC



Successive Approximation ADC



Flash ADC

5.RESULT : The operation of all converter is studied.

6.PRECAUTIONS :

1.connections should be tight.

2. power supply should be turned on after checking supply.